Extended Temperature Range Supplement

3341/3341A 64 x 4 FIFO Serial Memory

MOS Memory Products

Description

The 3341 or 3341A is a 64-word x 4-bit First-In First-Out (FIFO) serial memory. Inputs and the outputs are completely independent (no common clocks) making the 3341/3341A ideal for asynchronous buffer applications.

Special on-chip input pull-up circuits and bipolar-compatible output buffers provide direct bipolar interfacing with no external components required. Control signals are provided for both vertical and horizontal cascading.

The 3341 and 3341A are manufactured using the p-channel Isoplanar silicon gate process and are available in both ceramic and plastic packages.

- **1 MHz (3341A) AND 700 kHz (3341) DATA RATES**
- **INDEPENDENT ASYNCHRONOUS INPUTS AND OUTPUTS**
- **FULLY TTL COMPATIBLE**
- **EXPANDABLE IN EITHER DIRECTION**
- **ACTIVE PULL-UP ON INPUTS**
- **TWO TEMPERATURE RANGES**
- **16-PIN DUAL IN-LINE PACKAGE**

Pin Names

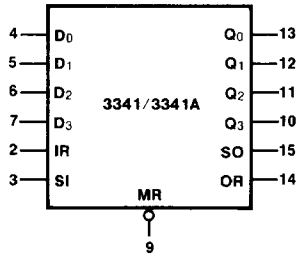
IR	Input Ready
SI	Shift In
D_0-D_3	Data Inputs
$\overline{MR}$	Master Reset
OR	Output Ready
SO	Shift Out
Q_0-Q_3	Data Outputs
V_{SS}	+5 V Power Supply
V_{DD}	0 V Power Supply
V_{GG}	−12 V Power Supply

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Operating Temperature	DL: −55°C to +85°C DM: −55°C to +125°C
Voltage on All Pins Except V_{DD} with Respect to V_{SS}	−20 V to +0.3 V
Voltage on V_{DD}	−7.0 V to +0.3 V

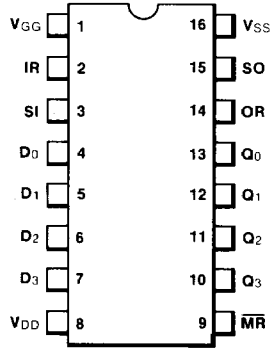
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 1

Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D

DC Characteristics V_{SS} = +5 V ± 5%, V_{GG} = −12 V ± 5%, V_{DD} = 0 V over full operating temperature range unless otherwise indicated

Symbol	Characteristic	F3341DL/DM, 3341ADL/DM Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{SS} −1.0			V	Notes 1 and 2
V_{IL}	Input LOW Voltage			0.8	V	Note 1
V_{OH}	Output HIGH Voltage	V_{SS} − 1.0			V	I_{OH} = −0.3 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 1.6 mA
V_{II}	Input Pull-up Initiation Voltage			2.0	V	V_{SS} = 4.75 V
				2.2	V	V_{SS} = 5.25 V
V_{IP}	Peak Input Current Voltage Point			V_{SS} − 1.5	V	
I_{IH}	Input HIGH Current	−200			μA	Note 1, V_{IN} = V_{SS} − 1.0 V
I_{IL}	Input Leakage Current			−50	μA	Note 1, V_{IN} = 0 V
I_{IP}	Input Barrier Current			−2.0	mA	Note 1
I_{GG}	V_{GG} Current			−16	mA	
I_{DD}	V_{DD} Current			−60	mA	

Notes

1. Inputs include D_0-D_3. Master Reset, Shift In, and Shift Out.
2. Internal pull-up circuits are provided on all inputs to insure proper HIGH level.
3. Control signals include Input Ready, Shift In, Output Ready, and Shift Out.
4. This parameter defines total time from the time data is loaded into the first word location to the time it is available at Q_0-Q_3 with the FIFO initially empty. Conversely, t_{BT} also defines the time required for an empty space to propagate from the last word location back to the first word location. When the FIFO is full, this is the time from the HIGH-to-LOW transition of OR to the LOW-to-HIGH transition of IR.
5. 1 TTL load +20 pF.
6. The $\overline{MR}$ input overrides all other control functions. It resets the control register and the input and output control logic while disabling any SI or SO inputs.
7. t_{IRH} is referenced to the positive going edge of IR or SI, whichever occurs later.
8. t_{IRL} is referenced to the negative going edge of IR or SI, whichever occurs later.
9. t_{DD} is referenced to the positive going edge of IR or SI, whichever occurs later.
10. t_{OVH} is referenced to the positive going edge of IR or SI, whichever occurs later.
11. t_{OVL} is referenced to the negative going edge of IR or SI whichever occurs later.
12. Data must be stable for t_{DH} or t_{IRH}, whichever is shorter.
13. t_{ORH} is referenced to the positive going edge of OR or SO, whichever occurs later.
14. t_{ORL} is referenced to the negative going edge of OR or SO, whichever occurs later.
15. t_{DV} is referenced to the negative going edge of OR or SO, whichever occurs later.
16. t_{OVH} is referenced to the positive going edge of IR or SI, whichever occurs later.
17. t_{OVL} is referenced to the negative going edge of IR or SI, whichever occurs later.

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AC Characteristics V_{CC} = +5 V ± 5%, V_{DD} = 0 V, V_{GG} = −12 V ± 5%
over full operating temperature range unless otherwise indicated

		3341A DL/DM			3341 DL/DM				
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Condition**
t_{IRH}	Input Ready HIGH Time	80		400	100	300	550	ns	Notes 7, 12
t_{IRL}	Input Ready LOW Time	100		550	138	300	550	ns	Note 8
t_{OVH}	Control Overlap HIGH Time	80			100			ns	Notes 3, 16
t_{OVL}	Control Overlap LOW Time	80			100			ns	Notes 3, 17
t_{DH}	Data Input Stable Time	200			400			ns	
t_{DD}	Data Input Delay Time			0			25	ns	Note 9
t_{ORH}	Output Ready HIGH Time	80		450	100	300	500	ns	Note 13
t_{ORL}	Output Ready LOW Time	80		550	170	450	850	ns	Note 14
t_{BT}	Data Bubble-through Time			16			32	μs	Note 4
t_{DV}	Data Valid After SO or OR	75			75			ns	Note 15
t_{MRW}	Master Reset Pulse Width	400			400			ns	Note 6
t_{DA}	Data Output Available Time	0			0			ns	
C_{IN}	Input Capacitance of Data and Control Lines			7.0			7.0	pF	f = 1 MHz, $V_{IN} = V_{SS}$
C_{MR}	Input Capacitance of $\overline{MR}$			7.0			15	pF	f = 1 MHz, $V_{MR} = V_{SS}$
f	Operating Frequency			1000			700	kHz	Note 5

Notes on previous page

For block diagram, functional description, timing diagrams and applications refer to standard 3341/3341A data sheet, Section 5.