# HF Receiver

# RA 1792
# (85830)

# Maintenance Manual


## Racal Communications Limited

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Prepared by Group Technical Handbooks Department, Racal Group Services Limited


RACAL
*The Electronics Group*


Ref. TH 3416

Printed in England

Issue 11
Feb. 87 — 200

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## HANDBOOK AMENDMENTS

Amendments to this handbook (if any), which are on coloured paper for ease of identification, will be found at the rear of the book. The action called for by the amendments should be carried out by hand as soon as possible.

## 'POZIDRIV' SCREWDRIVERS

Metric thread cross-head screws fitted to Racal equipment are of the 'Pozidriv' type. Phillips type and 'Pozidriv' type screwdrivers are not interchangeable, and the use of the wrong screwdriver will cause damage. POZIDRIV is a registered trademark of G.K.N. Screws and Fasteners Limited. The 'Pozidriv' screwdrivers are manufactured by Stanley Tools Limited.

## FOREWORD

Operating Instructions for the RA 1792 will be found in the Operators Manual for the HF Communications Receiver System RA 1792/MA 1075 Ref TH 2184.

RA 1792

## OPTIONS

When options are fitted or changed subsequent to manufacture, it may be necessary to fit revised PROMS, carrying the applicable software programme, to the Microcomputer Board. It is advisable to consult Racal Communications Limited prior to field fitment of options.

RACAL
TH 3416

Overall View, RA1792 Receiver

# RA 1792 - HF RECEIVER

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## TECHNICAL SPECIFICATION

| | |
|---|---|
| Frequency Range | 150 kHz to 30 MHz |
| Modes of Reception | USB/LSB (R3E, H3E, J3E, R2A, H2A, J2A)<br>AM (A3E)<br>MCW (A2A)<br>CW (A1A)<br>ISB (B8E) optional<br>FM (F3E)<br>Auxiliary - provides demodulated signal centred on optional fixed BFO offset frequency. |
| Tuning | Continuously tunable sythesizer in 10 Hz steps over the entire frequency range. Frequency setting either by numerical keypad or by single tuning knob with continuously variable tuning rate from 1 kHz per turn to approximately 20 kHz per turn, depending on the speed of rotation. |
| Pre-programmed Channels | EAROM memory unit may be programmed with up to 100 channel frequencies and mode which may be recalled by keypad or tuning control. |
| Channel Scanning | Automatic scanning of up to ten channels in any decade of the 100 stored channels. Dwell time on each channel variable in ten steps from 0.1 to 10 seconds; pre-selected by numeric keypad. |
| Frequency Stability | Dependent upon frequency standard used:<br>1. The following optional internal standard may be supplied:<br>(a) Temperature Compensated Crystal Oscillator (TCXO): ±2 in $10^6$ from -10°C to +55°C.<br>(b) Type 9442:<br>(i) Temperature: ±3 in $10^9$/°C<br>(ii) Long term: ±3 in $10^9$ per day after 3 months continuous operation.<br>2. External standard input: 1 MHz, 5 MHz, or 10 MHz level 0 dBm into 50 ohms. |
| Antenna Input | (a) Wideband, 50 ohms to 75 ohms nominal.<br>(b) The receiver will withstand without damage input signals of 50 V EMF continuously.<br>(c) Re-radiation:<br>(i) 0 to 30 MHz; not greater than 10μV PD<br>(ii) 30 to 100 MHz: not greater than 200 pW |

Sensitivity

(a) CW and SSB (A1A, R2A, A3E, R3E, J3E): In a 3 kHz bandwidth, signal-plus-noise to noise ratio is better than: 150 kHz to 1 MHz: 10 dB with 3 µV (EMF) input, 1 MHz to 30 MHz: 10 dB with 1 µV (EMF) Input.

(b) AM (A3E): In a 6 kHz bandwidth, signal-to-noise to noise ratio is better than: 150 kHz to 1 MHz: 10 dB with 10 µV (EMF) input, 70% modulated at 1 kHz, 1 MHz to 30 MHz: 10 dB with 3 µV (EMF) input, 70% modulated at 1 kHz.

IF Selectivity

USB: +250 Hz to +3.2 kHz at -6 dB
-400 Hz to +4.3 kHz at -60 dB

LSB: -250 Hz to -3.2 kHz at -6 dB
+400 Hz to -4.3 kHz at -60 dB

CW1: 300 Hz at -6 dB
3 kHz at -60 dB

CW2: 1 kHz at -6 dB
6 kHz at -60 dB

AM1: 3.2 kHz at -6 dB
12 kHz at -60 dB

AM2: 6.0 kHz at -6 dB
20 kHz at -60 dB

AM3: 16 kHz at -6 dB
50 kHz at -60 dB

Note: A maximum of six filters may be installed, in addition to a 16 kHz bypass.

Cross Modulation

With a wanted signal of 1 mV EMF in a 3 kHz bandwidth, an unwanted signal 30 % modulated removed not less than 20 kHz, must be greater than 500 mV EMF to produce an output 20 dB below the output produced by the wanted signal.

Reciprocal Mixing

With a wanted signal of less than 100 µV EMF in a 3 kHz bandwidth, an unwanted signal more than 20 kHz removed is generally greater than 65 dB above the wanted signal level to give a noise level 20 dB below the output produced by the wanted signal.

Blocking

With a wanted signal of 1 mV EMF, an unwanted signal more than 20 kHz removed must be greater than 1 V EMF to reduce the output by 3 dB.

Intermodulation Products

(a) In band:
Two 100 mV EMF signals within the IF passband will produce third order intermodulation products not greater than -50 dB relative to the level of either tone at the IF output.

| | |
|---|---|
| | (b) Out of band:<br>With two 30 mV EMF signals, separated and removed from the wanted signal by not less than 25 kHz, the third order intermodulation products are not less than 90 dB below either of the interfering signals. |
| Spurious Responses | (a) External (including image and IF rejection):<br>External signals, removed more than 20 kHz from the wanted frequency, must be greater than +80 dB relative to 1 µV EMF to produce an output equal to that produced by a 1 µV EMF signal at the wanted frequency. |
| | (b) Internal:<br>The presence of an internally generated spurious response generally will not degrade the specified receiver sensitivity by more than 3 dB. |
| AGC | (a) Range:<br>An increase in input level of 110 dB above 2 µV EMF will produce an output change of less than 2 dB. |
| | (b) Time constants:<br>Short, medium and long - preset to be automatically selected by mode switching, but can be set independently by push-buttons. AGC lines are available at rear of receiver to permit remote control. |
| IF Gain Control | Control range 110 dB:<br>Gain control may be switched either to manually set receiver gain or AGC threshold. |
| BFO | (a) Variable by main tuning control, ±8 kHz, synthesized in 10 Hz steps. |
| | (b) Pre-selected fixed offsets may be selected for use with external demodulator. |
| Pre-set Operating Conditions | Bandwidth, AGC time constant, and BFO offset may be preset for each mode so that they are automatically recalled when the mode is selected.<br><br>'Auxiliary' mode may be set up for any mode, bandwidth, AGC time constant and BFO offset. In the ISB mode, different AGC time constants may be stored for the two sidebands. |
| 1st LO Output | 10 dBm ±3 dBm into 50 ohm load, on rear panel. |
| IF Output | 455 kHz, nominal 100 mV into 50 ohms. |
| Muting | 60 dB minimum by grounding rear panel connection. |

| | |
|---|---|
| AF Output | (a) Line output, 10 mW maximum into 600 ohms balanced, adjustable by internal preset level control.<br><br>(b) Phone output, 1 mW maximum into 600 ohms unbalanced.<br><br>(c) 200 mW maximum to internal loudspeaker which may be switched in or out of operation.<br><br>(d) Connection for external loudspeaker, 200 mW into 16 ohms; 400 mW into 8 ohms. |
| Metering | Front panel display switched to indicate RF level or AF level output to line. |
| BITE | All measured supply voltages to be within ±20%<br><br>Varactor line voltage:-<br>20 MHz Reference Loop: 6 to 11 V DC<br>BFO Synthesizer: 8 V ±0.5 V DC<br>LO Synthesizer: 3.5 to 15 V |
| Power Supply | AC: Selections for 110, 120, 220, or 240 V operation; +10% -15%. 45 to 65 Hz. DC: Receiver may also be operated from an 18 to 32 V dc source when receiver is equipped with optional dc power supply. |
| Power Consumption | Approximately 60 VA for ac operation; approximately 40 Watts for dc operation. |
| Display Illumination | Presettable (See Chapter 11). |
| Environmental Conditions | (a) The equipment is designed to operate under the following climatic conditions:<br>Operating temperature $-10^{o}C$ to $+55^{o}C$<br>Storage temperature $-40^{o}C$ to $+70^{o}C$<br>Relative humidity 95% at $+40^{o}C$<br><br>(b) The equipment is suitable for mobile operation.<br><br>(c) The equipment is suitable for air transportation in unpressurized conditions and for operation up to altitudes of 3500 metres above sea level. |
| Dimensions | Height - 133 mm (5.25 in.)<br>Width - 483 mm (19 in.)<br>Depth - 458 mm (18 in.) |
| Weight | 14 kg (31 lbs). |

# CHAPTER 1

# GENERAL DESCRIPTION

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# CHAPTER 1

# GENERAL DESCRIPTION

## INTRODUCTION

1. This chapter briefly describes the RA1792 receiver incorporating BITE (Built in Test Equipment). For detailed information, reference should be made to the appropriate chapters in this manual.

## RA1792 RECEIVER

2. The RA1792 is a fully synthesized programmable communications receiver, covering the frequency range 150KHz to 30MHz in 10Hz steps. Frequency selection is achieved either through the use of a keypad or through the use of a single rotary tuning control. The receiver is also equipped with a 100 channel memory. Each channel may be preset to a particular operating frequency and mode using the front panel controls. When a particular channel is selected, the receiver will instantly tune to the preset frequency and mode parameters. The receiver may also be set to the SCAN mode; in this mode, the receiver will automatically scan ten (or less) selected channels, stopping for a preset dwell time (0.1 to 10 seconds) at each channel.

3. Reception of CW(A1A), MCW(A2A), AM(A3E), USB/LSB (R3E, H3E, J3E, R2A, H2A, J2A) and FM(F3E) modes is provided as standard, with ISB(B8E) available as an option.

## Table 1.1 Radio Emission Codes

Radio Emission Codes are specified using three symbols as shown below:-

First symbol - Type of modulation of main carrier
Second symbol - Nature of modulating signal
Third symbol - Nature of transmitted signal

The principal symbols are listed below:-

| First Symbol | Type of Modulation |
|---|---|
| A | Double sideband, AM |
| B | Independent sideband, AM |
| C | Vestigial sideband, AM |
| D | Amplitude/Angle modulation |
| F | Frequency modulation |
| G | Phase Modulation |
| H | Single sideband full carrier |
| J | Single sideband suppressed carrier |
| K | Pulses, amplitude modulated |
| L | Pulses, width or duration modulated |
| M | Pulses, phase or position modulated |
| N | Unmodulated carrier |
| P | Pulses, unmodulated |
| R | Singleside band reduced or variable carrier |
| | |
| Second Symbol | Nature of Modulation Signal |
| 0 | No modulation signal |
| 1 | On/Off modulation (keyed CW) |
| 2 | Modulation sub carrier (keyed MCW) |
| 3 | Analogue modulation (voice) |
| 7 | Two or more channels on one frequency offering keyed telegraphy |
| 8 | Two or more channels on one frequency offering telephony (voice) |
| | |
| Third Symbol | Type of Information being Transmitted |
| A | Telegraphy for aural reception |
| B | Telegraphy for automatic reception |
| C | Facsimile |
| D | Telemetry |
| E | Telephony |

4. The unit includes a battery-operated memory retention circuit to retain the frequency and all other receiver settings during a temporary supply failure.

Brief Technical Description

5. A block diagram of the RA1792 receiver is given in fig. 1.1. A received signal induced into the antenna is applied via a protection and muting circuit to a wide band RF amplifier stage, followed by a 30MHz low-pass filter. The protection circuit contains a relay which automatically open-circuits the RF path for signals at the antenna greater than approximately 5V e.m.f., or when a 0V mute signal is applied to the receiver via a rear panel connection or via the SCORE data. The low-pass filter protects the receiver from image frequency signals and also attenuates first local oscillator re-radiation from the antenna connection. The wide-band RF amplifier stage may be bypassed if not required. The normal operating frequency range of the receiver is from 150 kHz to 30 MHz. The receiver may however, be tuned to any frequency between zero and 30 MHz, although the receiver may not meet specification when tuned to frequencies below 150 kHz.

First Mixer

6. In the first mixer the received signal is combined with the 40.605 MHz to 70.455 MHz output signal from the first local oscillator 20 MHz reference loop, and the difference frequency signal, at 40.455 MHz, is applied via a 16 kHz roofing filter to the automatic gain controlled first IF amplifier. The first local oscillator synthesizer receives a 1 MHz reference frequency input from the second local oscillator/BFO synthesizer, and is set to the required frequency, in 10Hz increments, by data from the control and display section. The first local oscillator output signal is also taken to a rear panel connector.

Second Mixer

7. The 40.455 MHz first IF output signal from the first mixer is applied to the second mixer board where it is amplified and then combined with a 40 MHz signal from the second local oscillator/BFO synthesizer board. The difference frequency output signal, at 455 kHz, is filtered and amplified before application to the main IF/AF board.

Second local Oscillator/BFO Synthesizer

8. The second local oscillator is phase-locked to a reference frequency input signal. This may be derived either from an optional 5 MHz temperature compensated crystal oscillator (TCXO) located on the synthesizer board, an optional 5 MHz frequency standard module (A11), or from an external unit connected to the REF IN/OUT socket on the receiver rear panel. Wire links fitted to the second local oscillator/BFO synthesizer board allow the use of a 1 MHz, 5 MHz or 10 MHz external reference input signal. Note that when operation from an external reference signal is required, the INT/EXT slide switch on the receiver rear panel must be set to the EXT position. When this switch is set to the INT position, a 5 MHz reference signal derived from the internal reference source (TCXO or A11) is available at the rear panel REF IN/OUT socket.

Main IF/AF Board

9. The main IF/AF board accomodates up to six 455KHz filters which provide the main receiver selectivity. In standard production receivers, four of these filters are symmetrical, with nominal bandwidths of 6KHz, 3KHz 1KHz and 300Hz, whilst the remaining two are sideband filters (nominal 3KHz). When the receiver is fitted with the optional ISB IF/AF board (A5), the ISB/SSB link connected to the output of the LSB filter must be set to the ISB position. Note that a link is fitted to the IF/AF board to allow the selection of a nominal 16KHz bandwidth, as determined by the characteristics of the roofing filter fitted to the first mixer board.

10. The output signal from the selected filter (main IF/AF board) is applied to an automatic gain controlled IF amplifier and is then routed to:

(a) The AGC detector, which produces the AGC voltage applied to the AGC amplifier on the second mixer board, and the AGC or manual gain control voltage applied to the 455KHz second IF amplifier. The local or remote manual IF gain control setting data and/or the SHORT, MED or LONG AGC selection data, is routed, in parallel form, to the AGC detector under software control. In ISB operation, the AGC voltage applied to the AGC amplifier on the second mixer board is proportional to the higher of the two sideband signals (hence the two-way interchange between the main and ISB AGC detectors). The diversity AGC output (together with the ISB diversity AGC output, where applicable) is applied to the metering circuit (para.12).

(b) An IF output drive amplifier which feeds the 455KHz main IF output socket on the rear panel.

(c) The ISB/SSB/CW/AM detector, and a switch which routes either the 455KHz $\pm$ 8KHz BFO signal (ISB, SSB or CW modes) or the 455KHz main IF signal (AM or FM modes) to the FM detector. Thus for ISB, SSB and CW modes, the IF signal is mixed with the BFO signal from the FM detector. For the FM mode, the IF signal is applied to a limiting amplifier and FM detector. In the AM mode, a limited carrier, i.e. the IF signal with the modulation removed, is produced by the FM detector and is applied to the ISB/SSB/CW/AM detector in place of the BFO signal.

11. The detected audio signals are routed to the appropriate audio output amplifiers by the software-controlled audio switching circuitry and preset line level controls. For SSB receivers (ISB IF/AF board not fitted) the audio line output is taken from the audio monitor amplifier. For ISB versions of the receiver, when the ISB mode is selected, the USB audio line output is taken from the line 1 amplifier, the LSB audio line output is taken from the line 2 amplifier, and the monitor line amplifier together with the loudspeaker audio amplifier is fed from either the USB or the LSB channel, as displayed on the front panel. When an ISB receiver is set for SSB operation, all four audio amplifiers are fed from the selected sideband.

12. The manual gain and metering circuits essentially consist of a digital to analogue converter to control the receiver IF gain (para 10 (a)), and an analogue to digital converter from which the front panel meter display is derived. The RF level indication is derived from the diversity AGC and/or the ISB diversity AGC input signals, whilst the AF level indication is taken from the output of the audio monitor line amplifier.

13. All command signals, whether from the front panel controls or from an extended remote operating position, are processed by the microprocessor assembly which includes non-volatile EAROMs located on the front panel memory board. These store pre-programmed frequency and mode information in each of 100 discrete channel locations for instant recall. Two separate buses carry control data and address information to/from the microprocessor/control assemblies to the synthesizers for frequency selection, and to the appropriate switching circuits controlling the different operating modes.

BITE

14. The receiver incorporates BITE (Built-in Test Equipment). This facility enables rapid assessment of the receivers operational status by means of a series of tests which are performed automatically after selection from the front panel operating controls. Information concerning the tests is shown on the front panel L.C.D. indicators, which are also checked as part of the tests.

15. BITE provides 34 tests which may be used by the operator or engineer, plus additional routines for use by engineers only. BITE may be called into operation at any time without affecting the programming of the receiver.

Tests are numbered in sequence starting at 0 and the numbers are shown on the left-hand liquid crystal display (LCD) in the position occupied by the channel number when the receiver is being used normally.

16. Table 1-2 is a condensed list of tests performed by BITE. Further details of the tests are given in Chapter 14.

TABLE 1-2 TESTS PERFORMED BY BITE

| TEST NO | TEST |
|---|---|
| 0-6 | Power Supplies |
| 7 | Display Test |
| 8-10 | Checks on the 3 types of memory fitted |
| 11 | *Reference Oscillator Varactor line voltage |
| 12 | *BFO varactor line voltage |
| 13 | *1st L.O. varactor line voltage and synthesizer sweep test |
| 14 | A3 AGC line Voltage |
| 15 | BFO Sweep test |
| 16-18 | Main IF AGC/MGC compatibility test |
| 19-20 | ISB IF AGC/MGC compatibility test |
| 21-26 | Filter tests |
| 27-28 | AM and FM detector tests |
| 29 | This is a prompt for manual connection of loopback connector, if SCORE board is fitted. |
| 30-33 | SCORE loopback test. |
| * | This parameter is also automatically checked during normal use. |

Additional routines for servicing purposes are listed in Chapter 14.

## MECHANICAL DESCRIPTION

17. A rigid, die-cast, full width chassis is used as the base for the main frame of the receiver. Mounted within compartments on the underside of this chassis are the mixer boards and the frequency generation system.

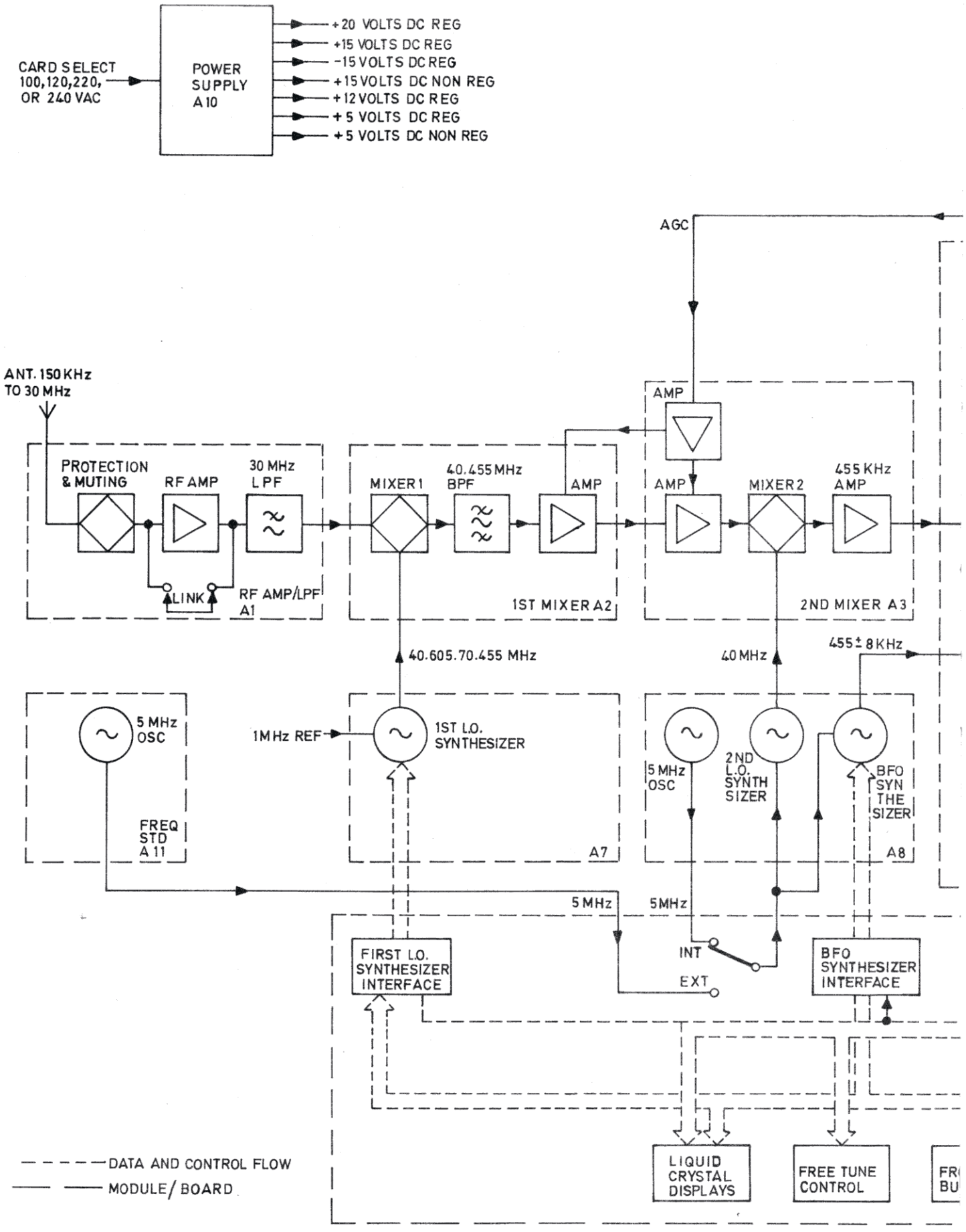
18. The input RF amplifier/low pass filter, main IF/AF, optional ISB IF/AF and power supply modules are located on the top surface of the cast chassis while the control and digital I/O modules are attached to the receiver main frame. All modules are accessible for maintenance and can be removed or replaced by the use of simple hand tools without the use of a soldering iron.

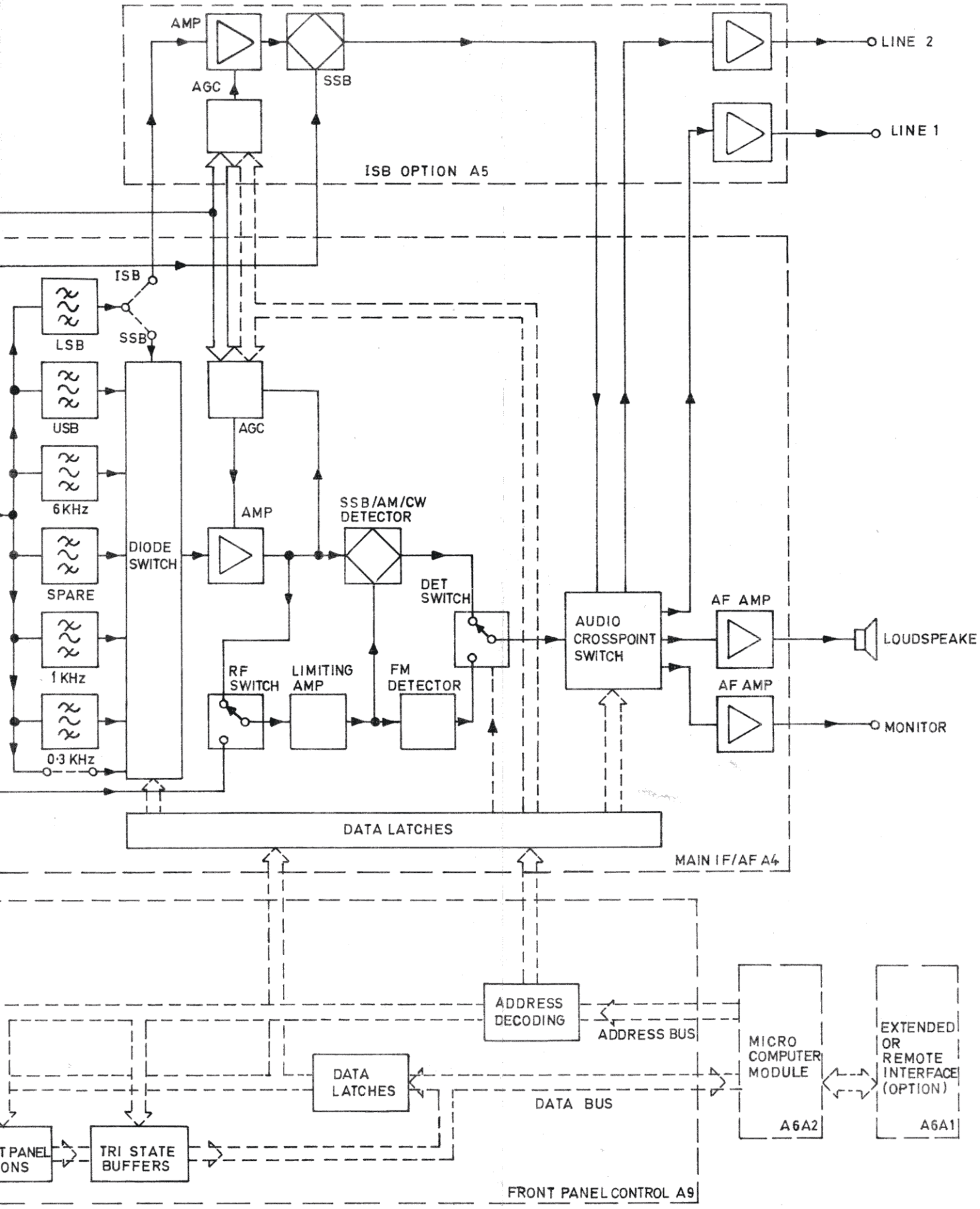
## REFERENCE DATA

19. Table 1-3 lists the different modules contained in the standard RA 1792 receiver, the available optional modules, and the Racal part number for each module.

TABLE 1-3 RECEIVER MODULES

| Designation | Module Name | Standard/ Optional | Part No. |
|---|---|---|---|
| A1 | Input RF Amplifier/Low Pass Filter | Standard | ST08076 |
| A2 | First Mixer Board | Standard | ST08184 |
| A3 | Second Mixer Board | Standard | ST08093 |
| A4 | Main IF/AF Board | Standard | ST82914 |
| A6A2 | Microcomputer Board | Standard | ST82912 |
| A7 | First LO Synthesizer | Standard | ST83733 |
| A8 | Second LO/BFO Synthesizer | Standard | ST82916 |
| A9A1 | Front Panel Switch & Display Board | Standard | ST08198 |
| A9A2 | Front Panel Memory Board | Standard | ST82920 |
| A10 | AC Power Supply Unit | Standard | ST80784 |
| A11 | Frequency Standard | Standard | ST08140 |
| A5 | ISB IF/AF Module | Optional | ST08109 |
| A6A1 | Remote Control SCORE Interface Module | Optional | ST08459 |
| A10 | DC Power Supply Module | Optional | ST80762 |


CARD SELECT
100,120,220,
OR 240 VAC
POWER
SUPPLY
A10
+20 VOLTS DC REG
+15 VOLTS DC REG
-15 VOLTS DC REG
+15 VOLTS DC NON REG
+12 VOLTS DC REG
+5 VOLTS DC REG
+5 VOLTS DC NON REG
AGC
ANT. 150 KHz
TO 30 MHz
PROTECTION
& MUTING
RF AMP
30 MHz
LPF
LINK
RF AMP/LPF
A1
MIXER 1
40.455 MHz
BPF
AMP
1ST MIXER A2
AMP
AMP
MIXER 2
455 KHz
AMP
2ND MIXER A3
40.605.70.455 MHz
40 MHz
455 ± 8 KHz
5 MHz
OSC
FREQ
STD
A11
1 MHz REF
1ST L.O.
SYNTHESIZER
A7
5 MHz
OSC
2ND
L.O.
SYNTH
SIZER
BFO
SYN
THE
SIZER
A8
5 MHz
5 MHz
FIRST L.O.
SYNTHESIZER
INTERFACE
INT
EXT
BFO
SYNTHESIZER
INTERFACE
LIQUID
CRYSTAL
DISPLAYS
FREE TUNE
CONTROL
DATA AND CONTROL FLOW
MODULE/BOARD




Overall Functional Diagram: RA 1792

Fig. 1.1

# CHAPTER 2

# RF AMPLIFIER/LPF MODULE A1

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| 2.1 | CIRCUIT: RF AMPLIFIER/LPF MODULE |
| 2.2 | COMPONENT LAYOUT: RF AMPLIFIER/LPF MODULE |

# CHAPTER 2

# RF AMPLIFIER/LPF MODULE A1

## INTRODUCTION

1. The RF Amplifier/LPF Module is comprised of receiver muting and RF input overload protection, followed by an optional RF amplifier which may be included or bypassed by connection of links. The RF signal then passes through a low pass filter before entering the next section, the First Mixer.

2. The following paragraphs describe circuit operation. The circuit diagram for this section is shown in figure 2-1, at the end of this chapter.

## CIRCUIT DESCRIPTION

3. The incoming RF signal passes from the antenna connector A1J1 over a lightning arrestor and through C1 and F1, a 1 Amp fuse for receiver protection. R1 and R2 establish the bias conditions for diodes CR1, CR2 and CR3. These diodes provide further input protection with CR2 additionally providing negative half-wave rectification of the input signal. This negative voltage is limited to 0.6 V below the 0 V (ground) rail and is smoothed over C3 before application to Q1.

4. R4 and R5 bias Q1 into conduction, energising RLA1. This closes contact RLA1 and allows the incoming RF signal to pass into the receiver.

5. If the incoming RF signal is greater than approximately 6 V rms, then the voltage provided by CR2 will turn off Q1, de-energising relay RLA1 thus disconnecting the RF Signal from the receiver. R6 discharges C3 quickly to allow for fast recovery from RF overload conditions.

6. External muting is provided by grounding J2C, which switches Q1 off via CR4. CR4 protects Q1 from the external application of positive voltages. Mute output is available on J2B.

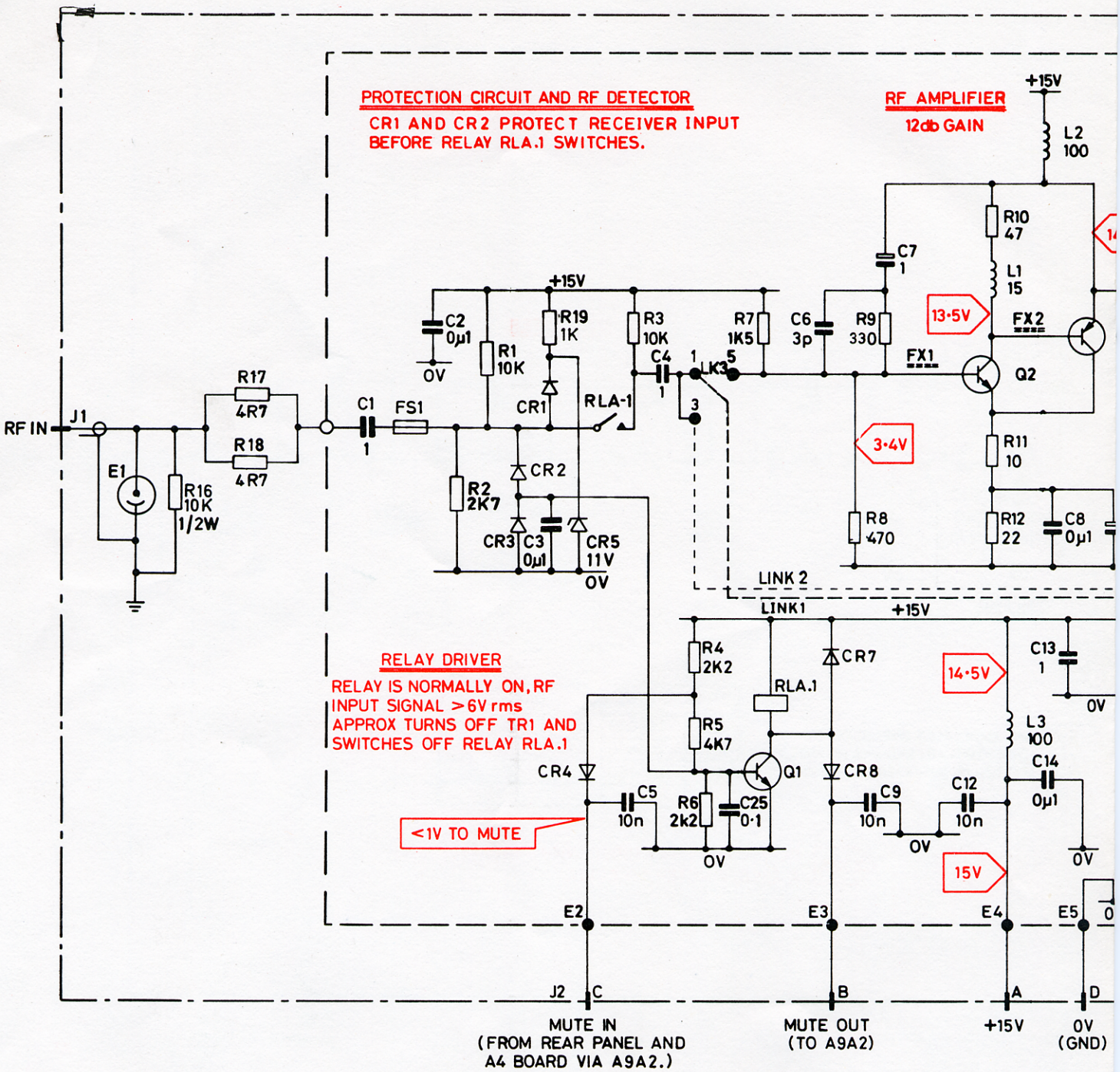
7. The RF signal is then passed through an optionally connected RF amplifier and then through a 4-section elliptical low pass filter which has a cut-off frequency of 35 MHz. The RF amplifier may be connected or by-passed by linking. The filter provides the necessary protection to the receiver from image signals at frequencies between 81.4 and 111.4 MHz, and from signals at the first intermediate frequency of 40.455 kHz. The filter also prevents first local oscillator reradiation from the antenna connection.

8. The RF amplifier has a fixed gain of 10 dB and consists of Q2 and Q3 in complementary configuration. The amplifier is bypassed when links LK1 and LK2 are fitted. The amplifier is in circuit when links LK3 and LK4 are fitted.

## RF AMPLIFIER/LPF BOARD A1 (ST 08078)

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R1 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R2 | 2.7 k | Metal Oxide | ¼ | 2 | 916548 |
| R3 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R4 | 2.2 k | Metal Oxide | ¼ | 2 | 916546 |
| R5 | 4.7 k | Metal Oxide | ¼ | 2 | 913490 |
| R6 | 2.2 k | Metal Oxide | ¼ | 2 | 916546 |
| R7 | 1.5 k | Metal Oxide | ¼ | 2 | 911166 |
| R8 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R9 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R10 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R11 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R12 | 22 | Metal Oxide | ¼ | 2 | 911627 |
| R13 | 270 | Metal Oxide | ¼ | 2 | 910391 |
| R14 | 18 | Metal Oxide | ¼ | 2 | 916545 |
| R15 | 270 | Metal Oxide | ¼ | 2 | 910391 |
| R16 | 10k | Carbon Composition | ½ | ±20 | 941490 |
| R17 | 4R7 | Carbon Composition | 1 | ±20 | 941489 |
| R18 | 4R7 | Carbon Composition | 1 | ±20 | 941489 |
| R19 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| **Capacitors** | | | V | | |
| C1 | 1 | Polyester | 100 | +20 -20 | 931163 |
| C2 | 0.1 | Ceramic | 50 | +20 -20 | 938406 |
| C3 | 0.1 | Ceramic | 50 | +20 -20 | 938406 |
| C4 | 1 | Ceramic | 100 | +20 -20 | 938401 |
| C5 | 0.01 | Ceramic | | +20 -20 | 938053 |
| C6 | 3.3 p | Silver Mica | 100 | ±¼pf | 941162 |
| C7 | 1 | Tantalum | 35 | +20 -20 | 938405 |
| C8 | 0.1 | Ceramic | 50 | +20 -20 | 938406 |
| C9 | 0.01 | Ceramic | | +20 -20 | 938053 |
| C10 | 6.8 | Tantalum | 35 | +20 -20 | 938030 |
| C11 | 1 | Ceramic | 100 | +20 -20 | 938401 |
| C12 | 0.01 | Ceramic | | +20 -20 | 938053 |
| C13 | 0.1 | Ceramic | 50 | +20 -20 | 938406 |
| C14 | 0.1 | Ceramic | 50 | +20 -20 | 938406 |
| C15 | 6.8 | Tantalum | 35 | +20 -20 | 938030 |
| C16 | 43 p | Silver Mica | | 2 | 943140 |
| C17 | 10 p | Silver Mica | | ±½pf | 943139 |
| C18 | 150 p | Silver Mica | 350 | 2 | 902238 |
| C19 | 75 p | Silver Mica | | ±1pf | 943141 |
| C20 | 110 p | Silver Mica | | ±1 | 943144 |

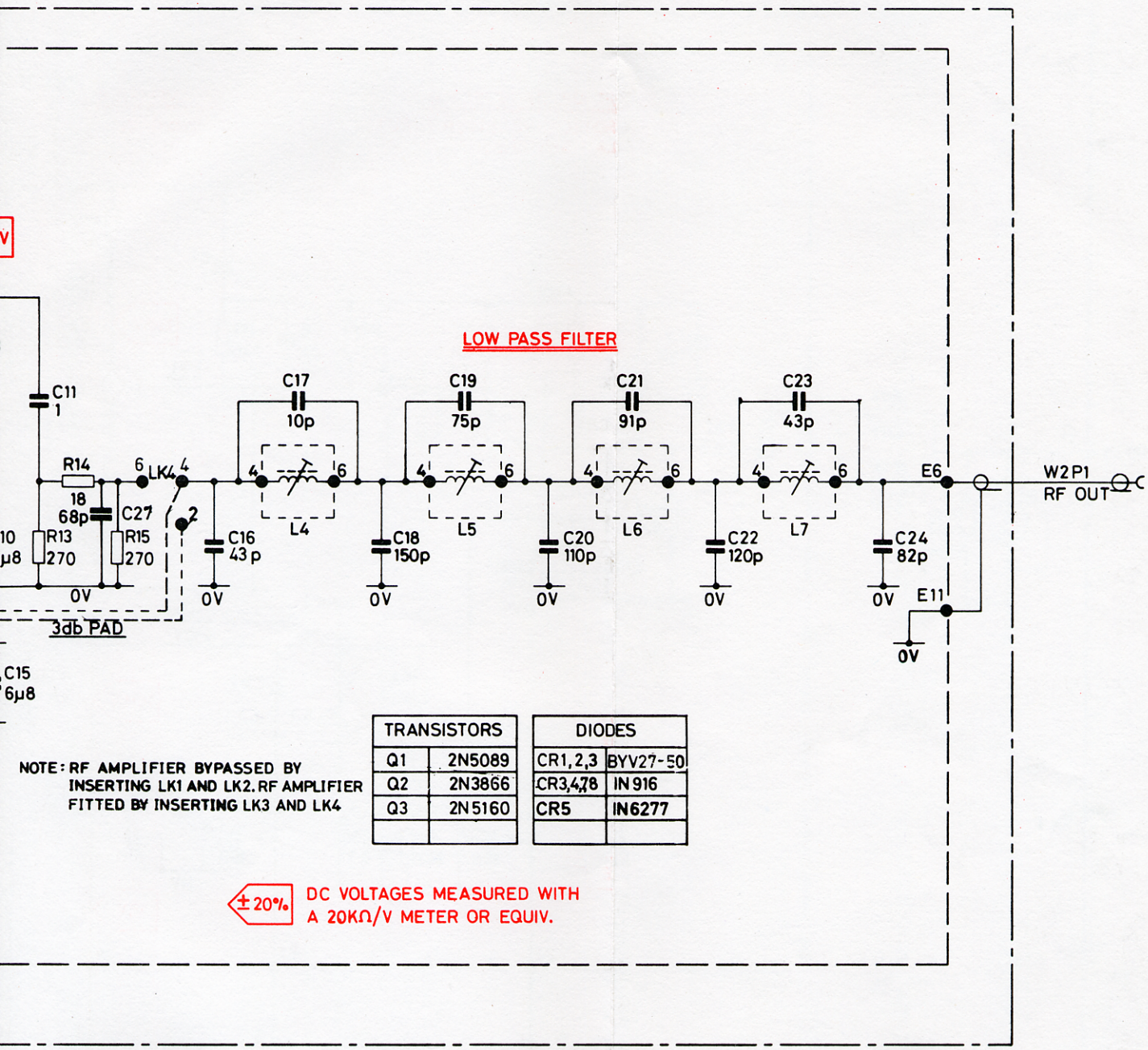
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| C21 | 91 p | Silver Mica | 500 | ±1pf | 943142 |
| C22 | 120 p | Silver Mica | 350 | 1 pf | 902236 |
| C23 | 43 p | Silver Mica | | ±1pf | 943140 |
| C24 | 82 p | Silver Mica | 350 | 2 | 902232 |
| C25 | 0.1 | Ceramic | 50 | 10 | 940318 |
| C26 | NOT USED | | | | |
| C27 | 68p | Ceramic | 50 | 10 | 940303 |
| **Diodes** | | | | | |
| CR1 | | BYV27-50 | | | 941848 |
| CR2 | | BYV27-50 | | | 941848 |
| CR3 | | BYV27-50 | | | 941848 |
| CR4 | | 1N916 | | | 913480 |
| CR5 | | 1N6277 | | | 941847 |
| CR6 | | Not used | | | |
| CR7 | | 1N916 | | | 913480 |
| CR8 | | 1N916 | | | 913480 |
| **Transistors** | | | | | |
| Q1 | | Silicon (2N5089) | | | 938417 |
| Q2 | | Silicon (2N3866) | | | 917219 |
| Q3 | | Silicon (2N5160) | | | 938418 |
| **Inductors** | | | | | |
| L1 | 15 µH | Choke | | | 915850 |
| L2 | 100 µH | Choke | | | 919471 |
| L3 | 100 µH | Choke | | | 919471 |
| L4 | | Coil, Variable | | | AT81393 |
| L5 | | Coil, Variable | | | AT81394 |
| L6 | | Coil, Variable | | | AT81395 |
| L7 | | Coil, Variable | | | AT81396 |
| **Miscellaneous** | | | | | |
| F1 | | Fuse, 1 Amp, ¼ x 5/8 Std Blo | | | 938415 |
| XF1 | | Fuse Holder | | | 938414 |
| FX1 | | Ferrite Bead | | | 907488 |
| FX2 | | Ferrite Bead | | | 907488 |
| K1 | | Relay, Reed 2 Form A | | | 938416 |
| A1J1 | | Socket, BNC (Ant. Input) | | | 938474 |
| A1J2 | | Plug, 4 pin | | | 938475 |
| | | Links (2 off) | | | 928478 |
| E1 | | Spark Arrester | | | 938761 |




RACAL

| TH1496 | DC08075/1 |
|---|---|
| 5 6 12 | |

| TH1496 | DC08075/2 |
|---|---|
| 5 12 | |




| TRANSISTORS | |
|---|---|
| Q1 | 2N5089 |
| Q2 | 2N3866 |
| Q3 | 2N5160 |
| | |

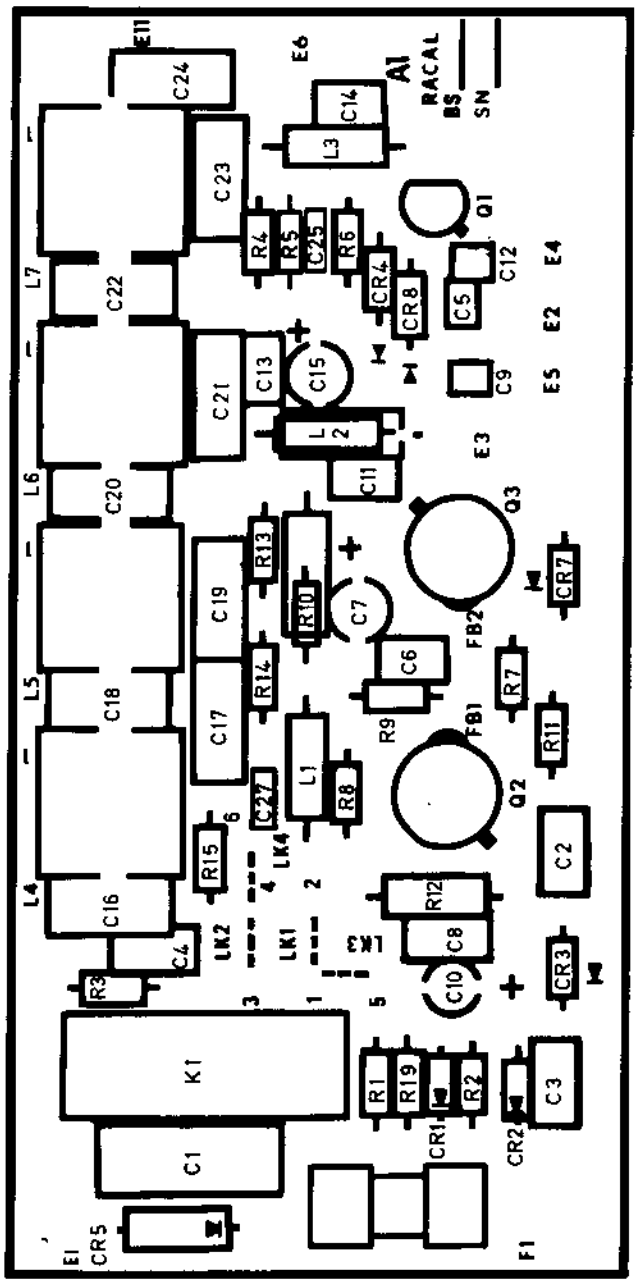
| DIODES | |
|---|---|
| CR1,2,3 | BYV27-50 |
| CR3,4,7,8 | IN 916 |
| CR5 | IN6277 |
| | |

NOTE: RF AMPLIFIER BYPASSED BY INSERTING LK1 AND LK2. RF AMPLIFIER FITTED BY INSERTING LK3 AND LK4

±20% DC VOLTAGES MEASURED WITH A 20KΩ/V METER OR EQUIV.

Circuit : RF Amplifier/ LPF Module A1

Fig. 2.1




Component Layout

RF Amplifier / Low Pass Filter Board A1 Fig. 2.2

# CHAPTER 3

# FIRST MIXER BOARD A2

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| Para | | Page |
|---|---|---|
| 1 | INTRODUCTION | 3-1 |
| | CIRCUIT DESCRIPTION | 3-1 |
| 2 | Signal Low Pass Filter and Mixer | 3-1 |
| 3 | Local Oscillator Input | 3-1 |
| 4 | Local Oscillator Drive Amplifier | 3-1 |
| 7 | First IF AGC | 3-2 |
| | COMPONENTS LIST | |


## ILLUSTRATIONS


| | |
|---|---|
| 3.1 | SIMPLIFIED BLOCK DIAGRAM: FIRST MIXER |
| 3.2 | CIRCUIT DIAGRAM: FIRST MIXER |
| 3.3 | COMPONENT LAYOUT: FIRST MIXER |

# CHAPTER 3

# FIRST MIXER BOARD A2

## INTRODUCTION

1. Figure 3-1 shows a simplified block diagram of the first mixer module A-2. It consists of a signal low pass filter, first mixer, roofing filter, first IF amplifier and drive amplifier with its associated filters. The function of this module is to convert the incoming RF signal to the first intermediate frequency of 40.455 MHz, by mixing with the local oscillator frequency of 40.605 to 70.455 MHz derived from the synthesizer. The circuit diagram of the first mixer is shown in Figure 3-2.

## CIRCUIT DESCRIPTION

### Signal Low Pass Filter and Mixer

2. The output from the A1 module is transferred to the first mixer through a 2 section elliptical low pass filter which has a cut-off frequency of 35 MHz. Link 2 permits isolation of the RF signal before it enters the mixer. The RF signal passes into the mixer via T1 and the local oscillator signal, after amplification, enters via T2. The mixer output is matched via T3 to the roofing filter, FL1, which selects the 40.455 MHz mixing product. The 3 dB bandwidth of this filter defines the widest bandwidth available in the receiver; 16 kHz. The mixer comprises T1, Q2, Q3, Q4, Q5 and T3.

### Local Oscillator Input

3. The local oscillator signal enters at J1 and can be monitored at TP1. The local oscillator signal then passes through a filter formed by L3, L4 and associated components. The signal may once again be monitored (TP2) before entering the local oscillator drive amplifier via R23.

### Local Oscillator Drive Amplifier

4. The local oscillator drive amplifier consists of Q6, Q7 and associated components. Q6 and Q7 are connected to form an antiphase stage driving into T2. The secondary of T2 provides the local oscillator input to the mixer.

5. Q6 and Q7 bases are biased to approx. 1.5 V. An incoming LO signal varies Q6 base voltage, producing an in-phase response at Q6 emitter. This is transferred via C17 to Q7 emitter. As Q7 base is at a fixed potential, variations at the emitter produce in-phase variations at Q7 collector, thus Q6 and Q7 collectors are in anti-phase.

6. The output of the mixer passes from T3 through FL1 to T4 via LK1. This link makes it possible to isolate succeeding receiver stages from the first mixer. The signal is then amplified by Q8. The output to the second mixer, the next stage in the receiver, is taken from a tap on transformer T5, which is in the load circuit of Q8.

First IF AGC

7. The AGC input, through A2J2 pin 6, controls the current through the PIN diode CR1, thus controlling the load impedance and consequently the gain of Q8. However, the linearity of this stage must remain high, so the gate bias of Q8 is varied by the bias signal through A2J2 pin 5 at the same time as the gain is being varied by the AGC signal. This ensures that sufficient current flows through Q8 to ensure high amplifier linearity.

## 1ST MIXER BOARD A2 (ST08184)

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R1 | | Not used | | | |
| R2 | | Not used | | | |
| R3 | | Not used | | | |
| R4 | | Not used | | | |
| R5 | | Not used | | | |
| R6 | | Not used | | | |
| R7 | | Not used | | | |
| R8 | 1.2 k | Metal Oxide | ¼ | 2 | 911179 |
| R9 | 150 | Metal Oxide | ¼ | 2 | 910389 |
| R10 | 100 k | Metal Oxide | ¼ | 2 | 915190 |
| R11 | 22 | Metal Oxide | ¼ | 2 | 920743 |
| R12 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R13 | 100 k | Metal Oxide | ¼ | 2 | 915190 |
| R14 | 22 | Metal Oxide | ¼ | 2 | 920743 |
| R15 | 1.2 k | Metal Oxide | ¼ | 2 | 911179 |
| R16 | 150 | Metal Oxide | ¼ | 2 | 910389 |
| R17 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R18 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R19 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R20 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R21 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R22 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R23 | 27 | Metal Oxide | ¼ | 2 | 920745 |
| **Capacitors** | | | V | | |
| C1 | 100 p | Silver Mica | 350 | 2 | 902234 |
| C2 | 43 p | Silver Mica | 350 | ±1pf | 943140 |
| C3 | 91 p | Silver Mica | 500 | ±1pf | 943142 |
| C4 | 390 p | Silver Mica | 350 | 2 | 902248 |
| C5 | 33 p | Silver Mica | 350 | 2 | 902222 |
| C6 | 100 p | Silver Mica | 350 | 2 | 902234 |
| C7 | 43 p | Silver Mica | 350 | ±1pf | 943140 |
| C8 | 150 p | Silver Mica | 350 | 2 | 902238 |
| C9 | 47 p | Silver Mica | 400 | 1 | 938834 |
| C10 | | Not Used | | | |
| C11 | 68 p | Silver Mica | 350 | 2 | 902230 |
| C12 | | Not Used | | | |
| C13 | | Not Used | | | |
| C14 | 680 p | Ceramic | | | 938479 |
| C15 | 0.1 | Ceramic | 50 | 20 | 938406 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| C16 | Not Used | | | | |
| C17 | 680 p | Ceramic | | | 938479 |
| C18 | 2.2 p | Ceramic | | | 938480 |
| C19 | 680 p | Ceramic | | | 938479 |
| C20 | 680 p | Ceramic | | | 938479 |
| C21 | | Not Used | | | |
| C22 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C23 | | Not Used | | | |
| C24 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C25 | 0.01 | Ceramic | | 20 | 938053 |
| C26 | 1000 p | Ceramic | | 20 | 938408 |
| *C27 | 27 p | Silver Mica | 350 | 2 | 902220 |
| C28 | 1000 p | Ceramic | | 20 | 938408 |
| C29 | 1000 p | Ceramic | | 20 | 938408 |
| C30 | 15 | Tantalum | 20 | 20 | 938034 |
| C31 | 0.01 | Ceramic | | 20 | 938053 |
| C32 | 1000 p | Ceramic | | 20 | 938408 |
| C33 | 1000 p | Ceramic | | 20 | 938408 |
| C34 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C35 | 0.01 | Ceramic | | 20 | 938053 |
| C36 | 0.01 | Ceramic | | 20 | 938053 |
| C37 | 27p | Silver Mica | 350 | 1p | 902220 |

*Earlier Versions 33 p 902222

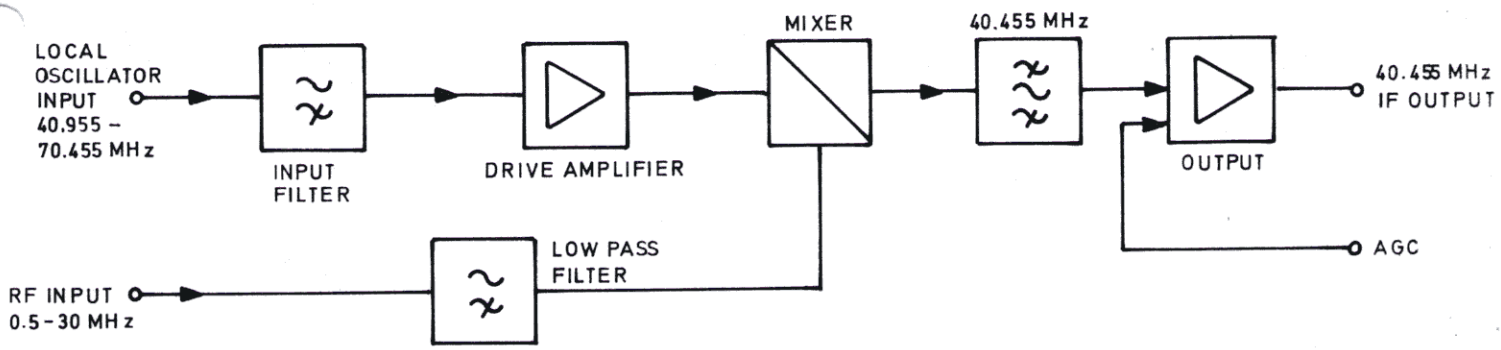
Diodes

| | | |
|---|---|---|
| CR1 | 5082-3080 | 921200 |

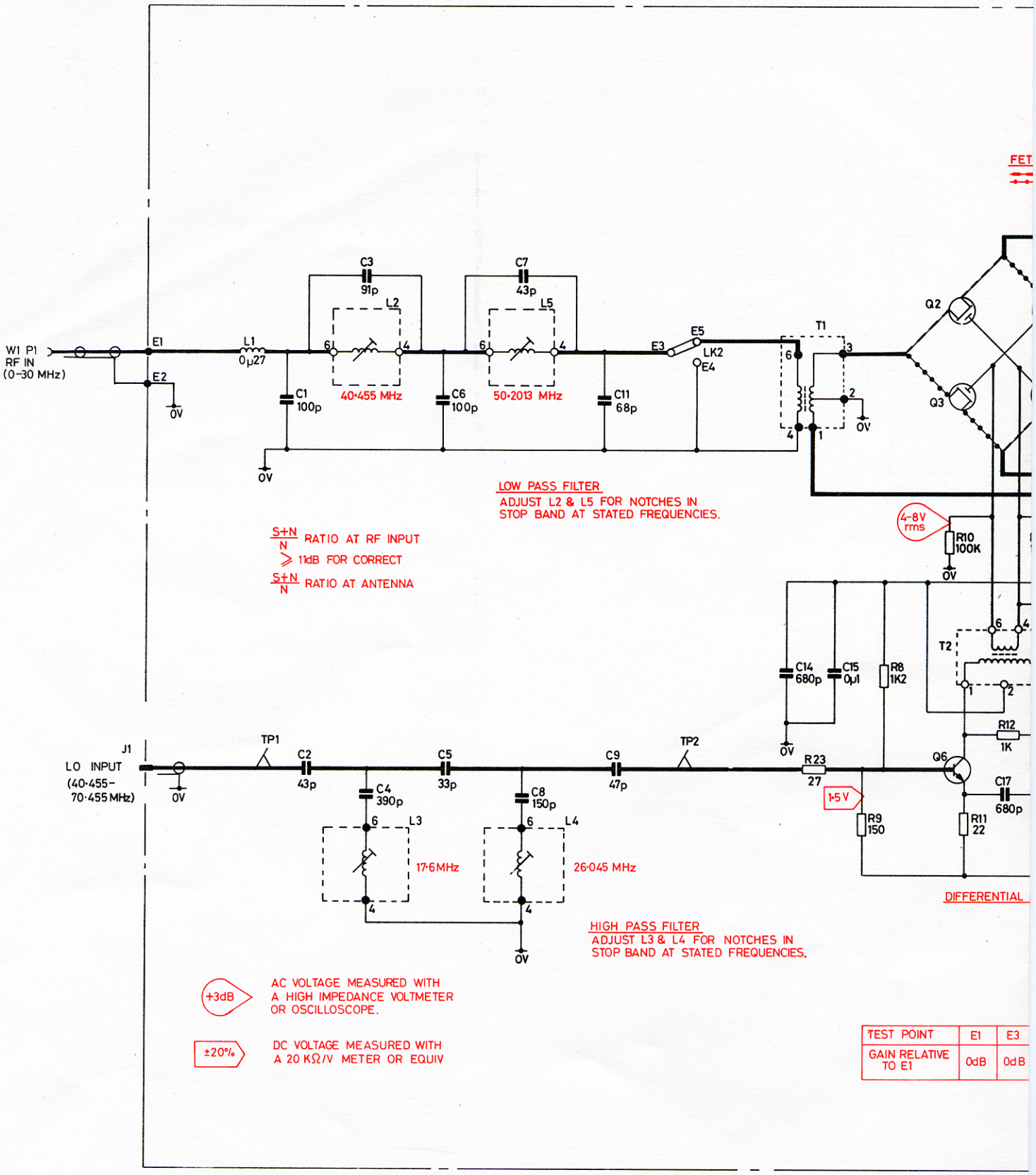
Transistors

| | | |
|---|---|---|
| Q1 | Not Used | |
| Q2 | Silicon (Matched BSV81) | A08298 |
| Q3 | Silicon (Matched BSV81) | A08298 |
| Q4 | Silicon (Matched BSV81) | A08298 |
| Q5 | Silicon (Matched BSV81) | A08298 |
| Q6 | Silicon (2N3866) | 917219 |
| Q7 | Silicon (2N3866) | 917219 |
| Q8 | Silicon (U310) | 932518 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Transformers** | | | | | |
| T1 | | RF Wide Band | | | AT81404 |
| T2 | | RF Wide Band | | | AT81405 |
| T3 | | RF Wide Band | | | AT81406 |
| T4 | | | | | AT81407 |
| T5 | | | | | AT81398 |
| **Inductors** | | | | | |
| L1 | 0.27µH | Choke RF | | | 938481 |
| L2 | | RF Variable Coil | | | AT81395 |
| L3 | | RF Variable Coil | | | AT81402 |
| L4 | | RF Variable Coil | | | AT81880 |
| L5 | | RF Variable Coil | | | AT81403 |
| L6 | | Variable Coil | | | AT83883 |
| L7 | | Not Used | | | |
| L8 | 10 µH | Choke | | | 921209 |
| L9 | 15 µH | Choke | | 10 | 915850 |
| L10 | 15 µH | Choke | | 10 | 915850 |
| **Connectors** | | | | | |
| J1 | | Plug, Coaxial RF | | | 938429 |
| J2 | | Plug, 8-way | | | B06846-4 |
| J3 | | Plug, Coaxial RF | | | 938429 |
| **Miscellaneous** | | | | | |
| FL1 | | 40.455 MHz Filter | | | BD80550 |




Simplified Block Diagram, First Mixer, A2 Fig.3-1

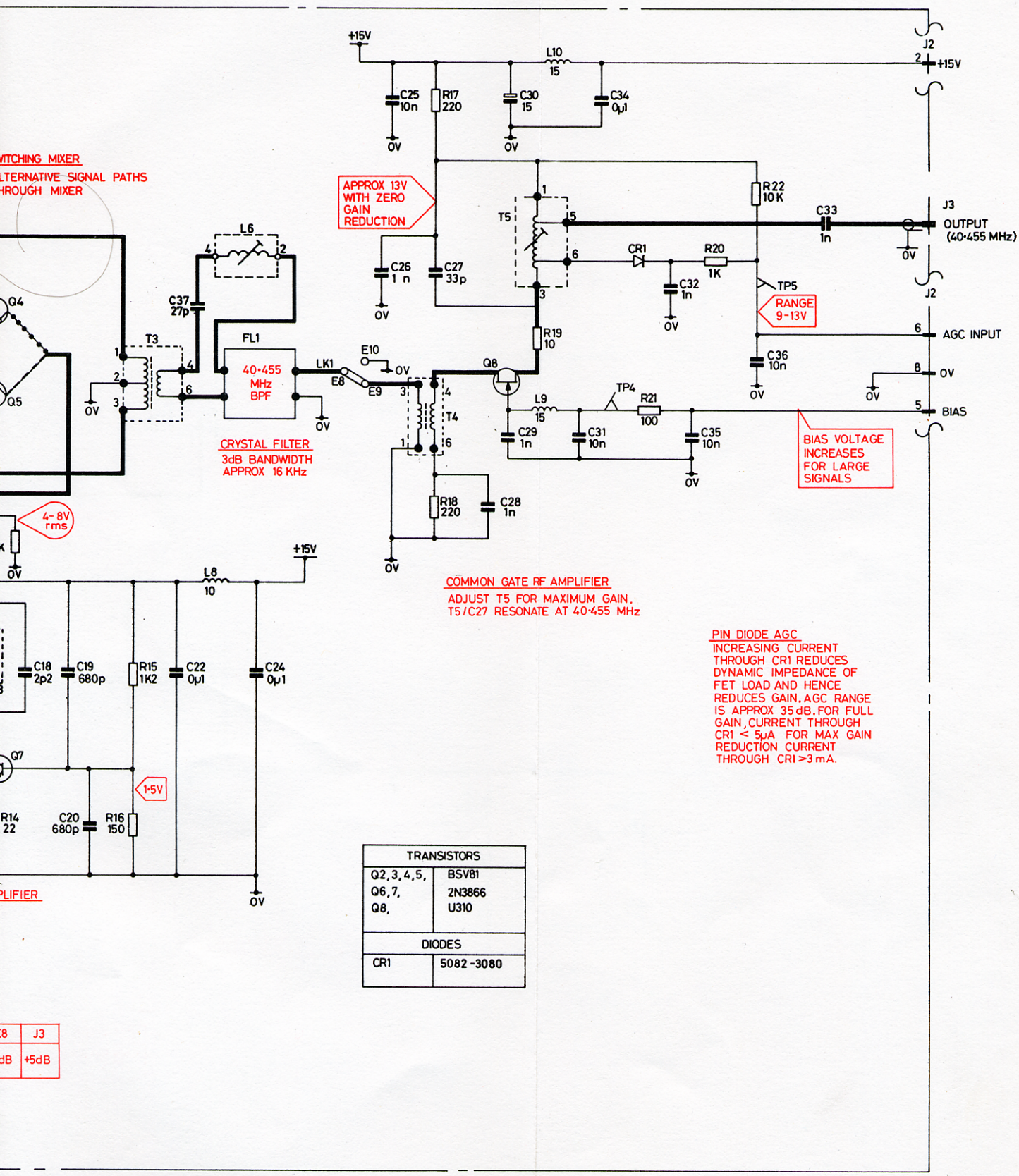



| TEST POINT | E1 | E3 |
|---|---|---|
| GAIN RELATIVE TO E1 | 0dB | 0dB |

RACAL

| TH3416 | DC08185/1 |
|---|---|
| 5 | 9 |

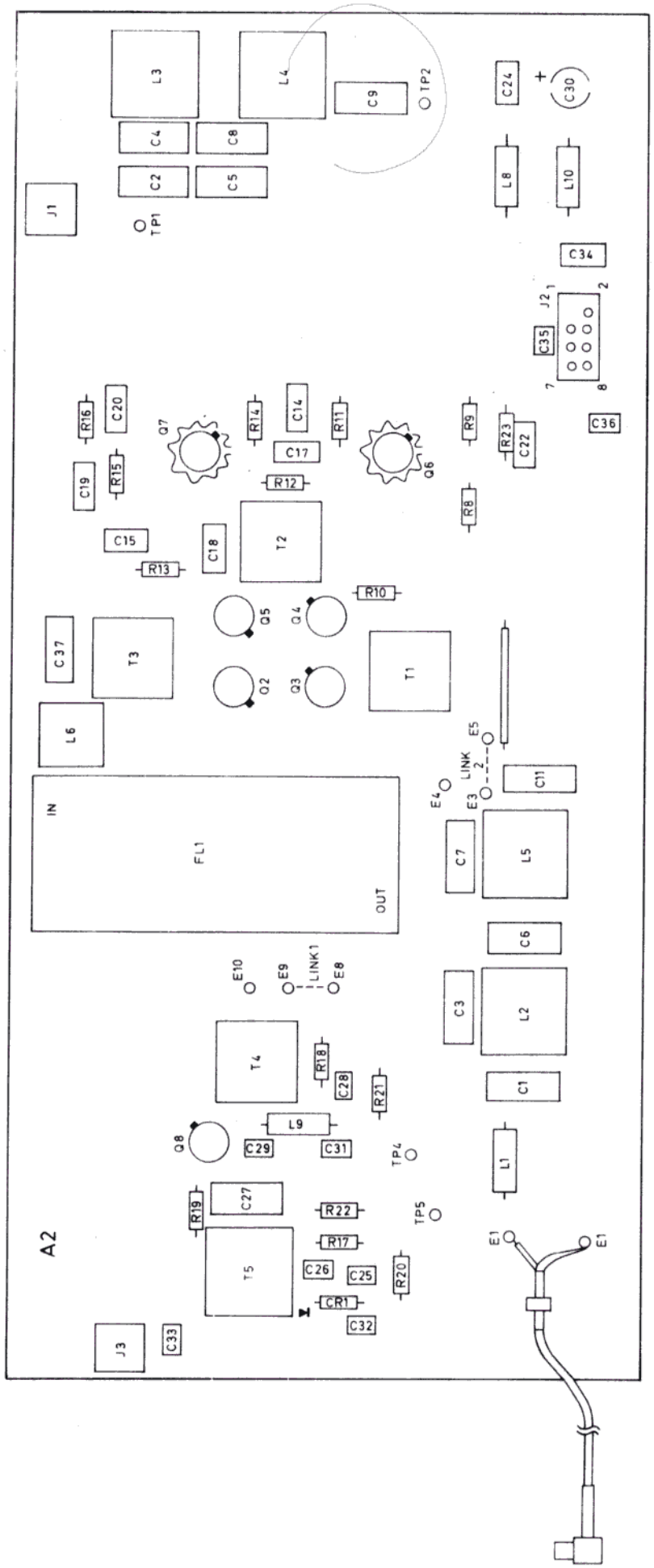
| TH3416 | DC08185/2 |
|---|---|
| 9 | |




| TRANSISTORS | |
|---|---|
| Q2, 3, 4, 5, Q6, 7, Q8, | BSV81 2N3866 U310 |
| **DIODES** | |
| CR1 | 5082-3080 |

| E8 | J3 |
|---|---|
| dB | +5dB |

**Circuit: First Mixer Module A2 Fig.3.2**




RACAL
TH1496 DO 8184
2 8

Component Layout: First Mixer Board, A2

Fig. 3.3

# CHAPTER 4

# SECOND MIXER BOARD A3

## CONTENTS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| 5 | Mixer | 4-1 |
| 6 | AGC | 4-1 |
| 8 | Bias | 4-1 |
| | COMPONENTS LIST | |


## ILLUSTRATIONS


| Fig. | |
|---|---|
| 4.1 | SIMPLIFIED BLOCK DIAGRAM: SECOND MIXER |
| 4.2 | CIRCUIT DIAGRAM: SECOND MIXER |
| 4.3 | COMPONENT LAYOUT: SECOND MIXER |

# CHAPTER 4

# SECOND MIXER BOARD A3

## INTRODUCTION

1. The Second Mixer, A3, contains three stages of amplification, filtering and a mixer. Additionally, circuitry is included which processes the AGC input on A3J1 pins 2 and 4 to provide AGC voltages for this mixer in addition to providing both bias and AGC voltages for the First Mixer amplifier, available on A3J1 pins 3 and 6 respectively.

2. A simplified block diagram is shown in Figure 4-1 and the circuit diagram is shown in Figure 4-2.

## CIRCUIT DESCRIPTION

### Input Amplification

3. The RF signal, now converted to 40.455 MHz, enters the board and is amplified by Q1, connected as a common gate amplifier. The output from this stage is taken from a tapping on T1, gain being controlled via PIN diode, CR1.

4. The signal is further amplified by Q2, a conventional common emitter stage driving into a four section bandpass filter tuned to 40.455 MHz.

### Mixer

5. The first IF signal from Q2 is applied to the signal port of the mixer U3. The 40 MHz second LO signal from A8 is applied via J2 to the mixer oscillator port. The difference signal of 455 kHz is selected at the mixer output by the tuned transformer T2 and the ceramic bandpass filter FL1. The output amplifier U4 provides a low impedance signal feed to the MAIN IF/AF module A4.

### AGC

6. The AGC voltage enters via A3J1 pins 2 and 4 and is applied to a circuit consisting of U2A, U1A, U1B, plus associated components, which converts a linear voltage change to a logarithmic current change. U2A acts as an amplifier whose negative feedback is affected by U1B, thus producing the logarithmic response. U1A, connected as part of the non-inverting input reference line for U2A, compensates for temperature variations in the circuit. This is possible because the transistors in U1 are formed on the same substrate, temperature changes affecting all equally. The output from U2A is applied via U1C to CR1, to control the gain of the first amplifier stage, Q1.

7. The output from U2A is also applied to U1D and to A3J1 pin 6 to provide gain control for the first mixer amplifier.

### Bias

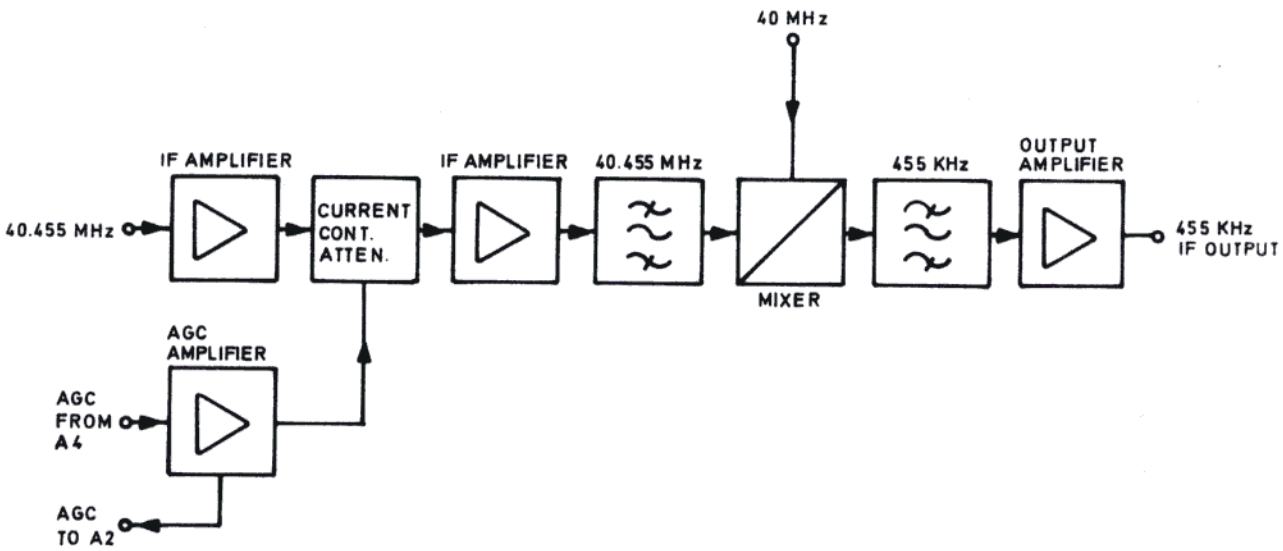
8. Bias for the first mixer amplifier is also provided from the A3 board. The AGC voltage from A3J1 pins 2 and 4 is inverted by U2B and buffered by U2C before leaving the A3 board via A3J1 pin 3.

## 2ND MIXER BOARD A3 (ST08093)

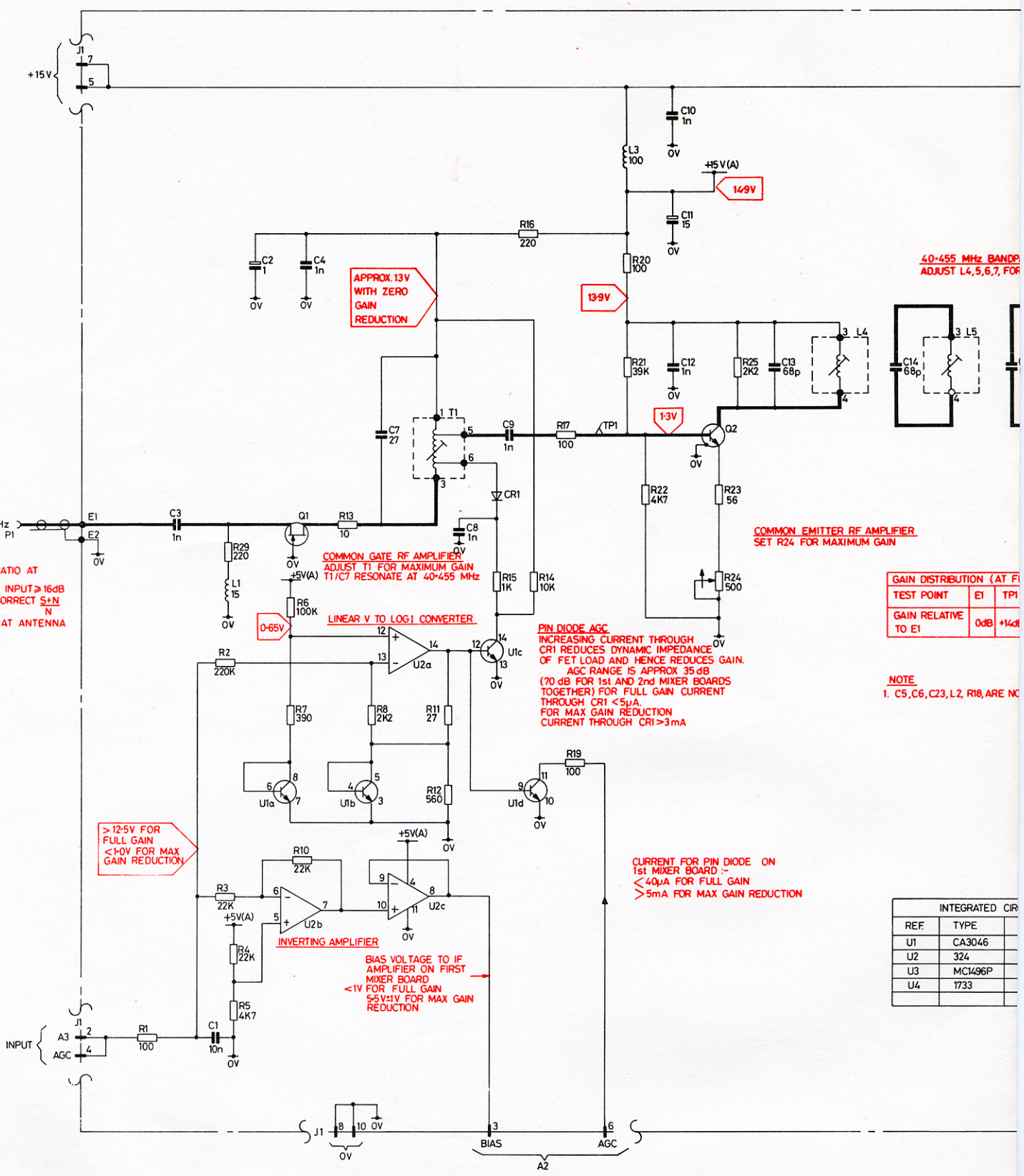
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | **W** | | |
| R1 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R2 | 220 k | Metal Oxide | ¼ | 2 | 921771 |
| R3 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R4 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R5 | 4.7 k | Metal Oxide | ¼ | 2 | 919490 |
| R6 | 100 k | Metal Oxide | ¼ | 2 | 915190 |
| R7 | 390 | Metal Oxide | ¼ | 2 | 916331 |
| R8 | 2.2 k | Metal Oxide | ¼ | 2 | 916546 |
| R9 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R10 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R11 | 27 | Metal Oxide | ¼ | 2 | 920745 |
| R12 | 560 | Metal Oxide | ¼ | 2 | 917061 |
| R13 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R14 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R15 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R16 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R17 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R18 | | Not Used | | | |
| R19 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R20 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R21 | 39 k | Metal Oxide | ¼ | 2 | 900993 |
| R22 | 4.7 k | Metal Oxide | ¼ | 2 | 919490 |
| R23 | 56 | Metal Oxide | ¼ | 2 | 917055 |
| R24 | 500 | Variable | | 20 | 941398 |
| R25 | 2.2 k | Metal Oxide | ¼ | 2 | 916546 |
| R26 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R27 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R28 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R29 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R30 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R31 | 39 | Metal Oxide | ¼ | 2 | 917062 |
| R32 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R33 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R34 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R35 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R36 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R37 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R38 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R39 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R40 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R41 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R42 | 47 | Metal Oxide | ¼ | 2 | 917063 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Capacitors** | | | V | | |
| C1 | 0.01 | Ceramic | | 20 | 938053 |
| C2 | 1 | Tantalum | 35 | 20 | 938405 |
| C3 | 1000 p | Ceramic | | 20 | 938408 |
| C4 | 1000 p | Ceramic | | 20 | 938408 |
| C5 | | Not used | | | |
| C6 | | Not used | | | |
| *C7 | 27 p | Silver Mica | 350 | 2 | 902220 |
| C8 | 1000 p | Ceramic | | 20 | 938408 |
| C9 | 1000 p | Ceramic | | 20 | 938408 |
| C10 | 1000 p | Ceramic | | 20 | 938408 |
| C11 | 15 | Tantalum | 20 | 20 | 938034 |
| C12 | 1000 p | Ceramic | | 20 | 938408 |
| C13 | 68 p | Silver Mica | 350 | 2 | 902230 |
| C14 | 68 p | Silver Mica | 350 | 2 | 902230 |
| C15 | 68 p | Silver Mica | 350 | 2 | 902230 |
| C16 | 82 p | Silver Mica | 350 | 2 | 902232 |
| C17 | 330 p | Silver Mica | 350 | 2 | 902246 |
| C18 | 1000 p | Ceramic | | 20 | 938408 |
| C19 | 1000 p | Ceramic | | 20 | 938408 |
| C20 | 1000 p | Ceramic | | 20 | 938408 |
| *Earlier Version | | 33p, 902222 | | | |
| C21 | 1000 p | Ceramic | | 20 | 938408 |
| C22 | 1 | Tantalum | 35 | 20 | 938405 |
| C23 | | Not used | | | |
| C24 | 0.1 | Ceramic | | 20 | 938406 |
| C25 | 0.1 | Ceramic | | 20 | 938406 |
| C26 | 15 | Tantalum | 20 | 20 | 938034 |
| C27 | 0.1 | Ceramic | | ±20 | 938406 |
| C28 | 15 | Tantalum | 20 | 20 | 938034 |
| C29 | 0.1 | Ceramic | | ±20 | 938406 |
| **Diodes** | | | | | |
| CR1 | | 5082-3080 | | | 921200 |
| **Transistors** | | | | | |
| Q1 | | Silicon (U310) | | | 932518 |
| Q2 | | Silicon (2N918) | | | 906517 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Integrated Circuits** | | | | | |
| U1 | | CA3046 | | | 922907 |
| U2 | | LM324N | | | 925944 |
| U3 | | MC1496P | | | 938427 |
| U4 | | MC1733 | | | 938428 |
| **Transformers** | | | | | |
| T1 | | RF Variable | | | AT81398 |
| T2 | | RF Variable | | | AT81399 |
| **Inductors** | | | | | |
| L1 | 15 µH | Choke RF | | | 915850 |
| L2 | | Not used | | | |
| L3 | 100 µH | Choke RF | | | 919471 |
| L4 | | Coil RF Variable | | | AT81397 |
| L5 | | Coil RF Variable | | | AT81397 |
| L6 | | Coil RF Variable | | | AT81397 |
| L7 | | Coil RF Variable | | | AT81397 |
| **Connectors** | | | | | |
| J1 | | Plug, 10-way | | | B06846-5 |
| J2 | | Plug, Coaxial RF | | | 938429 |
| **Miscellaneous** | | | | | |
| FL1 | | Filter VTD-3-A | | | 938425 |

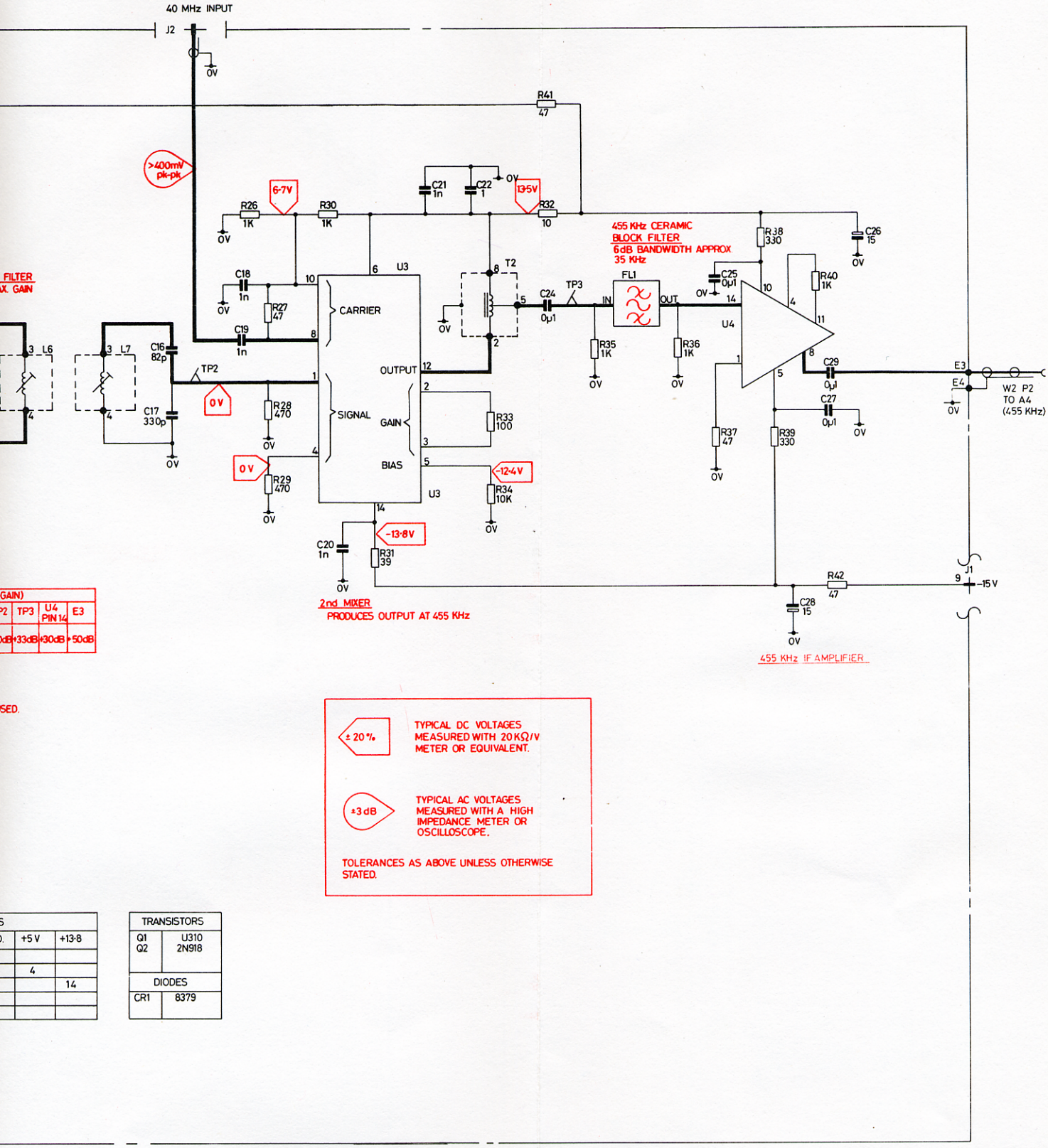



Simplified Block Diagram, Second Mixer, A3 Fig. 4-1




RACAL

| TH1495 | DC08082/1 | TH1496 | DC08082/2 |
|---|---|---|---|
| 5 | | 5 | |



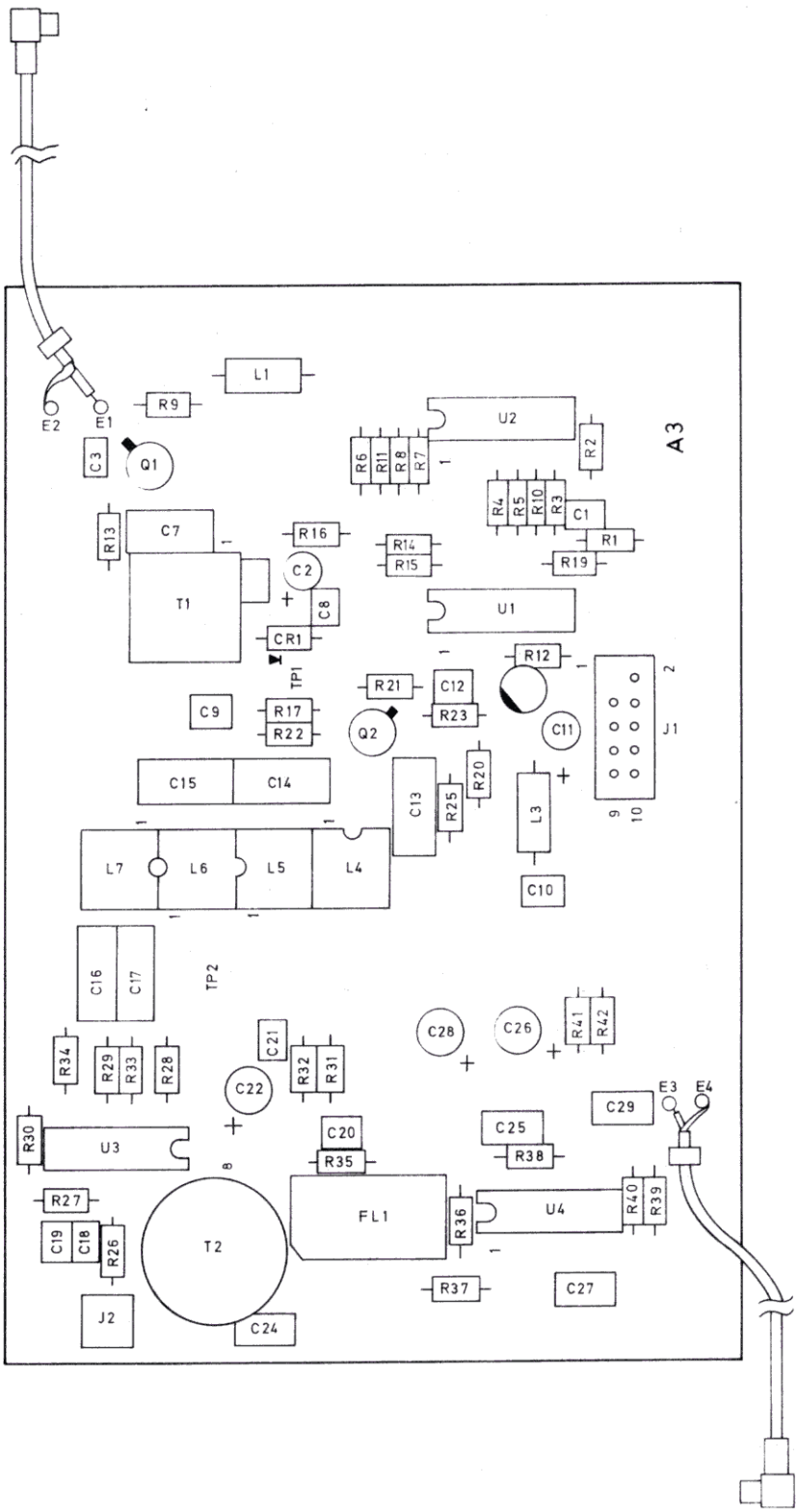

| GAIN) | | | |
|---|---|---|---|
| P2 | TP3 | U4 PIN 14 | E3 |
| 0dB | +33dB | +30dB | +50dB |

SED.

| S | | |
|---|---|---|
| ). | +5 V | +13·8 |
| | | |
| | 4 | |
| | | 14 |
| | | |
| | | |

| TRANSISTORS | |
|---|---|
| Q1<br>Q2 | U310<br>2N918 |
| DIODES | |
| CR1 | 8379 |

Circuit: Second Mixer Module A3 Fig. 4.2




RACAL
TH3416 CE08093
3

Component Layout : Second Mixer Board, A3

Fig.4.3

# CHAPTER 4

# SECOND MIXER BOARD A3

## INTRODUCTION

1. The Second Mixer, A3, contains three stages of amplification, filtering and a mixer. Additionally, circuitry is included which processes the AGC input on A3J1 pins 2 and 4 to provide AGC voltages for this mixer in addition to providing both bias and AGC voltages for the First Mixer amplifier, available on A3J1 pins 3 and 6 respectively.

2. A simplified block diagram is shown in Figure 4-1 and the circuit diagram is shown in Figure 4-2.

## CIRCUIT DESCRIPTION

### Input Amplification

3. The RF signal, now converted to 40.455 MHz, enters the board and is amplified by Q1, connected as a common gate amplifier. The output from this stage is taken from a tapping on T1, gain being controlled via PIN diode, CR1.

4. The signal is further amplified by Q2, a conventional common emitter stage driving into a four section bandpass filter tuned to 40.455 MHz.

### Mixer

5. The first IF signal from Q2 is applied to the signal port of the mixer U3. The 40 MHz second LO signal from A8 is applied via J2 to the mixer oscillator port. The difference signal of 455 kHz is selected at the mixer output by the tuned transformer T2 and the ceramic bandpass filter FL1. The output amplifier U4 provides a low impedance signal feed to the MAIN IF/AF module A4.

### AGC

6. The AGC voltage enters via A3J1 pins 2 and 4 and is applied to a circuit consisting of U2A, U1A, U1B, plus associated components, which converts a linear voltage change to a logarithmic current change. U2A acts as an amplifier whose negative feedback is affected by U1B, thus producing the logarithmic response. U1A, connected as part of the non-inverting input reference line for U2A, compensates for temperature variations in the circuit. This is possible because the transistors in U1 are formed on the same substrate, temperature changes affecting all equally. The output from U2A is applied via U1C to CR1, to control the gain of the first amplifier stage, Q1.

7. The output from U2A is also applied to U1D and to A3J1 pin 6 to provide gain control for the first mixer amplifier.

### Bias

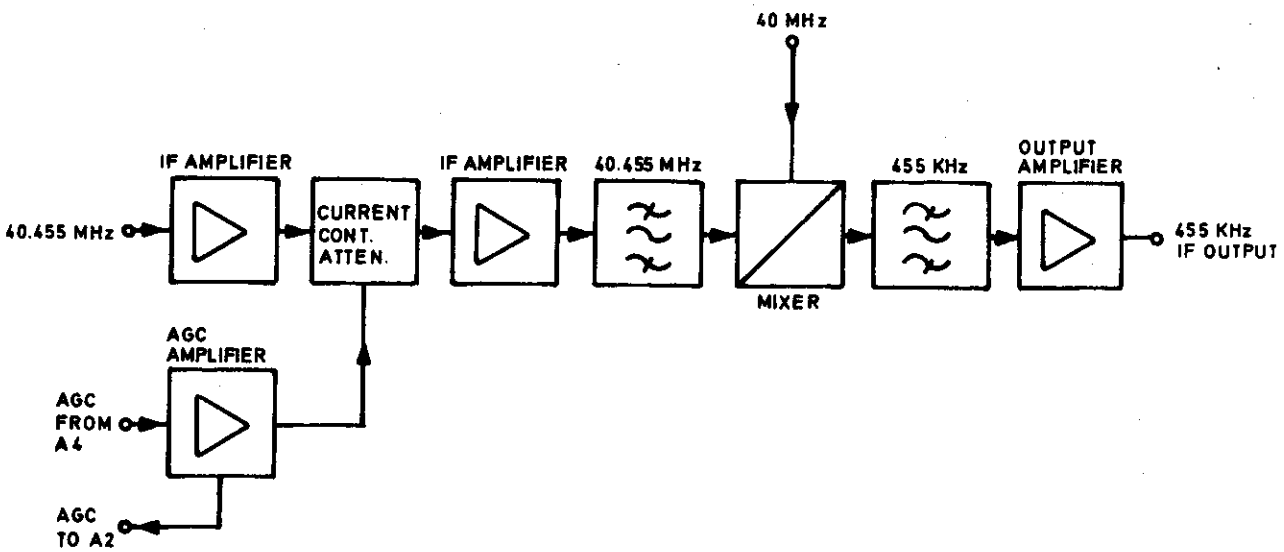
8. Bias for the first mixer amplifier is also provided from the A3 board. The AGC voltage from A3J1 pins 2 and 4 is inverted by U2B and buffered by U2C before leaving the A3 board via A3J1 pin 3.

## 2ND MIXER BOARD A3 (ST08093)

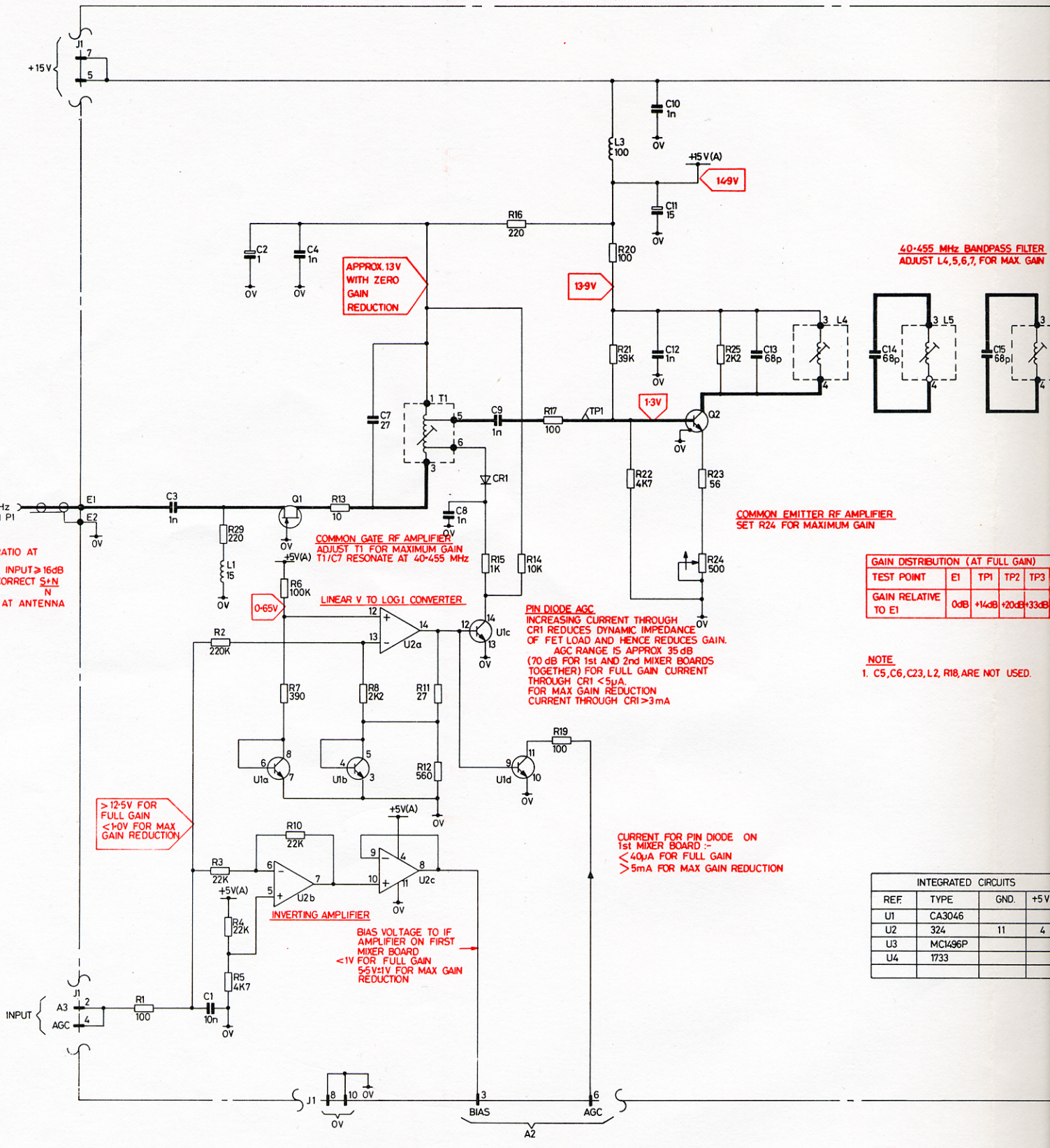
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | **W** | | |
| R1 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R2 | 220 k | Metal Oxide | ¼ | 2 | 921771 |
| R3 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R4 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R5 | 4.7 k | Metal Oxide | ¼ | 2 | 919490 |
| R6 | 100 k | Metal Oxide | ¼ | 2 | 915190 |
| R7 | 390 | Metal Oxide | ¼ | 2 | 916331 |
| R8 | 2.2 k | Metal Oxide | ¼ | 2 | 916546 |
| R9 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R10 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R11 | 27 | Metal Oxide | ¼ | 2 | 920745 |
| R12 | 560 | Metal Oxide | ¼ | 2 | 917061 |
| R13 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R14 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R15 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R16 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R17 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R18 | | Not Used | | | |
| R19 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R20 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R21 | 39 k | Metal Oxide | ¼ | 2 | 900993 |
| R22 | 4.7 k | Metal Oxide | ¼ | 2 | 919490 |
| R23 | 56 | Metal Oxide | ¼ | 2 | 917055 |
| R24 | 500 | Variable | | 20 | 941398 |
| R25 | 2.2 k | Metal Oxide | ¼ | 2 | 916546 |
| R26 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R27 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R28 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R29 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R30 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R31 | 39 | Metal Oxide | ¼ | 2 | 917062 |
| R32 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R33 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R34 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R35 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R36 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R37 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R38 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R39 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R40 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R41 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R42 | 47 | Metal Oxide | ¼ | 2 | 917063 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Capacitors** | | | V | | |
| C1 | 0.01 | Ceramic | | 20 | 938053 |
| C2 | 1 | Tantalum | 35 | 20 | 938405 |
| C3 | 1000 p | Ceramic | | 20 | 938408 |
| C4 | 1000 p | Ceramic | | 20 | 938408 |
| C5 | | Not used | | | |
| C6 | | Not used | | | |
| *C7 | 27 p | Silver Mica | 350 | 2 | 902220 |
| C8 | 1000 p | Ceramic | | 20 | 938408 |
| C9 | 1000 p | Ceramic | | 20 | 938408 |
| C10 | 1000 p | Ceramic | | 20 | 938408 |
| C11 | 15 | Tantalum | 20 | 20 | 938034 |
| C12 | 1000 p | Ceramic | | 20 | 938408 |
| C13 | 68 p | Silver Mica | 350 | 2 | 902230 |
| C14 | 68 p | Silver Mica | 350 | 2 | 902230 |
| C15 | 68 p | Silver Mica | 350 | 2 | 902230 |
| C16 | 82 p | Silver Mica | 350 | 2 | 902232 |
| C17 | 330 p | Silver Mica | 350 | 2 | 902246 |
| C18 | 1000 p | Ceramic | | 20 | 938408 |
| C19 | 1000 p | Ceramic | | 20 | 938408 |
| C20 | 1000 p | Ceramic | | 20 | 938408 |
| *Earlier Version 33p, 902222 | | | | | |
| C21 | 1000 p | Ceramic | | 20 | 938408 |
| C22 | 1 | Tantalum | 35 | 20 | 938405 |
| C23 | | Not used | | | |
| C24 | 0.1 | Ceramic | | 20 | 938406 |
| C25 | 0.1 | Ceramic | | 20 | 938406 |
| C26 | 15 | Tantalum | 20 | 20 | 938034 |
| C27 | 0.1 | Ceramic | | ±20 | 938406 |
| C28 | 15 | Tantalum | 20 | 20 | 938034 |
| C29 | 0.1 | Ceramic | | ±20 | 938406 |
| **Diodes** | | | | | |
| CR1 | | 5082-3080 | | | 921200 |
| **Transistors** | | | | | |
| Q1 | | Silicon (U310) | | | 932518 |
| Q2 | | Silicon (2N918) | | | 906517 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Integrated Circuits** | | | | | |
| U1 | | CA3046 | | | 922907 |
| U2 | | LM324N | | | 925944 |
| U3 | | MC1496P | | | 938427 |
| U4 | | MC1733 | | | 938428 |
| **Transformers** | | | | | |
| T1 | | RF Variable | | | AT81398 |
| T2 | | RF Variable | | | AT81399 |
| **Inductors** | | | | | |
| L1 | 15 µH | Choke RF | | | 915850 |
| L2 | | Not used | | | |
| L3 | 100 µH | Choke RF | | | 919471 |
| L4 | | Coil RF Variable | | | AT81397 |
| L5 | | Coil RF Variable | | | AT81397 |
| L6 | | Coil RF Variable | | | AT81397 |
| L7 | | Coil RF Variable | | | AT81397 |
| **Connectors** | | | | | |
| J1 | | Plug, 10-way | | | B06846-5 |
| J2 | | Plug, Coaxial RF | | | 938429 |
| **Miscellaneous** | | | | | |
| FL1 | | Filter VTD-3-A | | | 938425 |

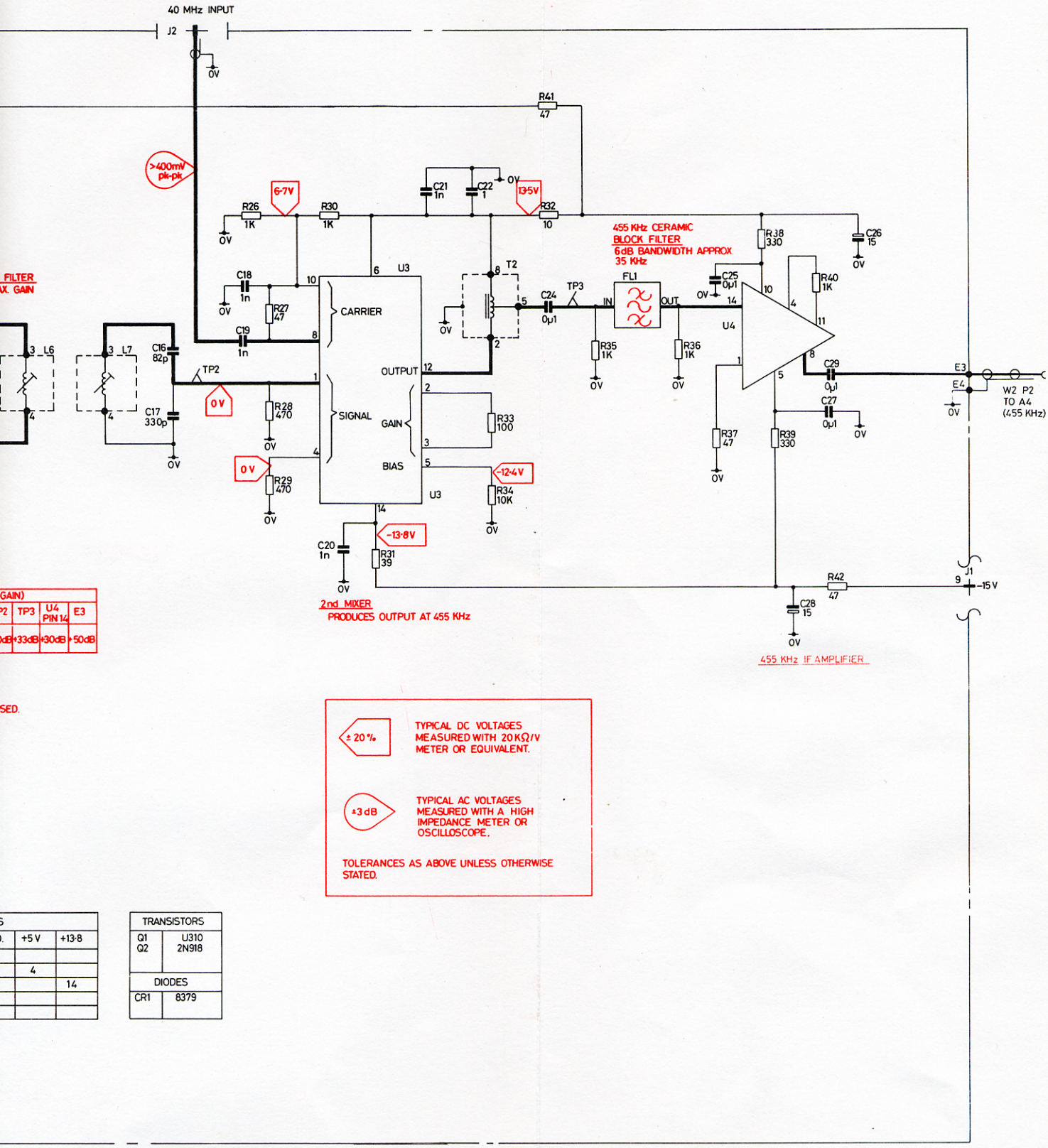



Simplified Block Diagram, Second Mixer, A3 Fig.4-1




RACAL

| TH1496 | DC08082/1 | TH1496' | DC08082/2 |
|---|---|---|---|
| 5 | | 5 | |



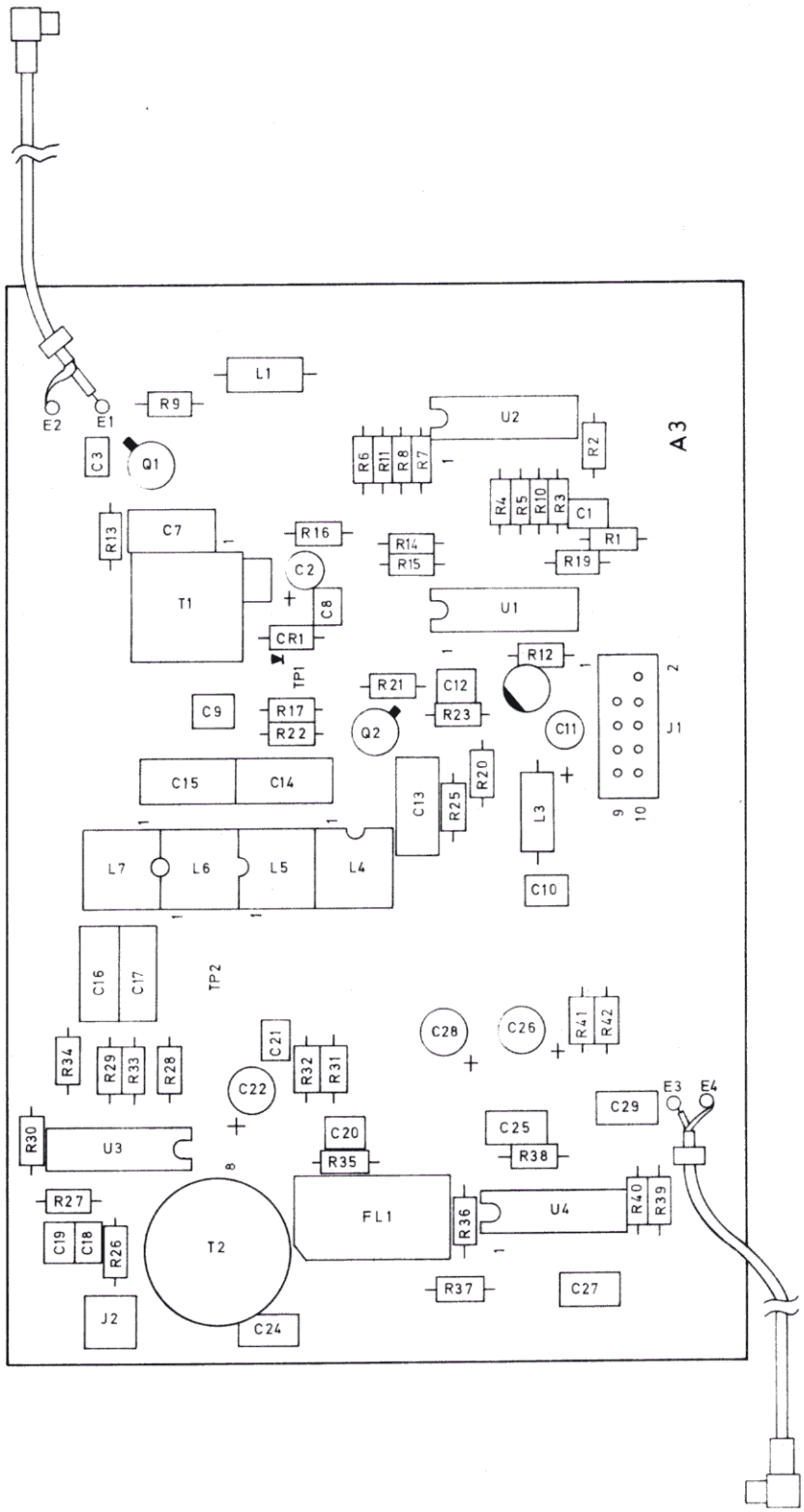

| GAIN) | | | |
|---|---|---|---|
| P2 | TP3 | U4 PIN 14 | E3 |
| dB | +33dB | +30dB | +50dB |

SED.

| S | | |
|---|---|---|
| ). | +5 V | +13·8 |
| | | |
| | 4 | |
| | | 14 |
| | | |
| | | |

| TRANSISTORS | |
|---|---|
| Q1<br>Q2 | U310<br>2N918 |
| DIODES | |
| CR1 | 8379 |

Circuit: Second Mixer Module A3 Fig. 4.2

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3

Component Layout : Second Mixer Board, A3

Fig.4.3

# CHAPTER 5

# MAIN IF/AF MODULE A4

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## ILLUSTRATIONS


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| 5.3 | COMPONENT LAYOUT: MAIN IF/AF MODULE |

# CHAPTER 5

# MAIN IF/AF MODULE A4

## INTRODUCTION

1. The Main IF/AF module A4 contains the 455 kHz filters used to determine the reception bandwidths, the second IF amplifier, the AM, FM and Product detectors with associated AF power amplifilers, together with the IF output and AGC circuits.

   Solid state switching circuits are also included for filter selection, detector selection, AGC time constants, remote gain control and signal level monitoring.

   Provision is also made for the necessary signal and control inputs to the optional ISB IF/AF module A5 when this facility is required.

   Figure 5-1 is a simplified diagram of the IF/AF module, figure 5-2 shows AGC voltage levels with HANG selected.

## IF FILTERS

2. The main IF/AF module will accommodate up to seven filters, five of these are normally symmetrical filters and two are sideband filters. When the 16 kHz bandwidth is selected these are bypassed and an attenuator is switched in to compensate for gain changes. When the 3 kHz bandwidth is selected the USB filter FL2, is switched in and the 1st LO synthesizer and bfo are offset by 1.7 kHz to make the USB filter appear symmetrical about the receiver frequency (unless optional 3 kHz symmetrical filter is fitted).

3. The required filter is selected by the binary coded logic inputs to A4J2, pin 35 (DB0), pin 31 (DB1), pin 33 (DB2) and pin 37 (DB3). DB0, 1, 2 and 3 represent the lower 4 bits of the microcomputer data bus and operate between 0 V (0) and +5 V (1). In order to select the chosen filter, the +5 V levels are shifted in U3 to +15 V, and are stored in U2 which is a 4-bit latch IC. The data is clocked into U2 by a positive going transition from U16. The data is then converted from BCD to decimal by U1, with the exception of the Q4 output of U2, which is taken directly to switch FL1 via R9, C21 and CR1. The output of filter FL1, when selected, may be sent to the main IF/AF signal path or the ISB IF (through J3) path (in the optional A5 card) by connection of link LK1 for the SSB or ISB mode.

4. The No. 1 output from U1 is set permanently high to disable the main IF when ISB is selected in an ISB receiver. U1 outputs 2-7 are used to select filters 2-7, assuming a full complement of filters has been fitted. The method of filter selection is similar to that used to select FL1.

AGC Controlled IF Amplifier

5. The source impedance of the signal from the selected filter is transformed from 5 K ohms to about 200 ohms by Q1 and the signal is then applied to an integrated circuit gain-controlled amplifier, U8. This device contains two amplifier sections which are connected in cascade to provide high gain and AGC range. The input signal is applied via C33 to pin 1, and the output from the first section, at pin 12, is applied via R39 and C40 to the input of the second section at pin 10. The output taken from pin 7 is applied via a bandpass filter to an emitter follower, Q6 and also to the IF output amplifier comprising Q7, Q8, Q9, and from there to the rear panel IF OUT connector, J2 at a level of 100 mV.

OPERATION OF AGC CIRCUITRY

6. The signal from the AGC controlled IF amplifiler (U8) is fed via Q6, which is connected as an emitter follower, to the AGC detector which comprises U10a, b and c. U10a and c provide an envelope of the audio signal available at TP3, whilst U10b provides thermal stability for U10c. The envelope is in the form of a DC voltage which may be sent on one of two paths, depending upon the AGC mode selected:

Peak AGC, used for USB, LSB and CW.

Carrier AGC, used for FM and AM (with short AGC decay).

The following paragraphs describe the operation of the AGC circuitry selected by peak AGC.

Peak AGC

7. The DC voltage following the audio envelope at TP3 passes into U7C, which detects the peak of the envelope. The peak voltage is then applied to the integrator, U14a, whose output falls with rising input peak values. The output voltage (which is available on TP8) is buffered by U17a and then passed to U17B. U17B inverts the voltage (available on TP11), which now rises with rising peak voltage. U17d acts with fast attack via R102 and CR28, and with slow decay via R103 and R101. The output of U17b is applied, via R51, to pins 3 and 4 of U8, hence controlling its gain. This loop represents the AGC control loop for the 2nd IF amplifier.

8. The basic AGC distribution is as follows. Initially, a voltage near the +15 V supply will be available on TP14, and the first IF amplifier gain is at maximum. R105 sets the threshold voltage at U17d, pin 5, allowing the voltage at TP11 to rise with increased signal strength, decreasing the second IF gain. The first IF gain remains at maximum becuase U17d pin 6 is still at a voltage below the threshold set on pin 5. Hence the second IF controls the receiver gain for the first 35 dB of signal increase above 2 µV.

9. As the signal strength continues to increase, the voltage on U17d, pin 6 increases until the voltage set up on pin 5 is reached and the voltage at TP14 now starts to decrease, reducing the gain of the first IF amplifier. This voltage is also fed back to U17b pin 12, which holds TP11 at a constant voltage. Continued increase in signal level reduces TP14 voltage whilst holding TP11 constant, so that for the next 70 dB, the gain is controlled by the 1st IF only.

10. As the signal strength increases over the last 5 dB of AGC range, TP14 reduces to zero volts, setting the 1st IF at minimum gain and allowing TP11 to increase in voltage, thereby further reducing the gain of the 2nd IF up to the limit of the AGC range. Hence the 2nd IF controls the last 5 dB of AGC range.

11. When peak AGC is selected, the decay time, as determined by R52 (and R53, R55, if switched in) is independent of attack time and follows the peak level.

Carrier AGC

12. For carrier AGC, U11b is open and Q5 is turned on by U15 via R59. This system decays through R44 and R54/C48 and the carrier level controls the AGC via R63 and U14a.

AGC Hang

13. A DC voltage representing the envelope of the audio waveform (output from the AGC detector) is applied to U7a pin 12. A threshold voltage is set up on pin 13 by R26 and R27. As the envelope voltage exceeds this threshold, C42 is charged, by pump action, via CR15. However, when a signal is present, U7b pin 9 is below the voltage of pin 10, so the output of U7b (TP4) is high, switching U10d on, and hence providing normal decay on the incoming signal.

14. With Hang selected (Q2 off) as soon as the signal disappears, the voltage at U7a pin 12 falls below the pin 13 threshold, so U7a pin 14 goes low, pulling U7b pin 10 below pin 9 which is held up by the charge on C42, so U7b pin 8 goes low, turning off U10d and the AGC 'hangs'. This continues until either C42 has discharged via R45 (which takes approximately 1.5 sec.), bringing the voltage at U7b pin 9 below that of pin 10, so turning on U7b and re-establishing the decay, or until the signal reappears, whereupon pin 10 voltage rises above that of pin 9, and decay is again resumed.

If Hang is not required, Q2 is on and any charge pumped through CR15 is grounded, thus preventing C42 from being charged.

AGC Dump

15. When the receiver is in Scan mode, the 'hang' is disabled momentarily during the frequency change, to enable a new signal level to establish the gains on the new frequency. This momentary disabling is known as 'AGC Dump', and operates as follows: Bit 4 on the databus carries a pulse through the voltage level shifter U5, to be clocked into U4, appearing at Q4 of this device. This in turn clocks U9 whose Q output switches on U10e, which pulls down the input to the integrator U14a. This increases receiver gain until a signal is established, which then resets the flip flop U9. The AGC dump also switches in a different charging path for C59, to maintain stability in the AGC filter.

Manual Gain

16. In the manual gain mode U11c and U12b are closed and the front panel IF gain sets up a voltage threshold at U14c pin 6. If the voltage at pin 5 is higher than the threshold at pin 6, then the output of U14c is high and is applied to the input of the integrator, U14a, which forces the integrator output lower, reducing the voltage at pin 5 and establishing a lower gain level. The same applies in reverse and hence a feedback loop is established to hold receiver gain at the threshold set by the manual gain control.

Manual IF Gain

17. The operator may manually select an AGC threshold via the front panel IF level control. In this mode U11c is closed and in conjunction with the IF gain control, sets the threshold. U11d is also closed to enable the D-A converter to provide control for signals of greater level than the manually set threshold. U12b is open, putting CR20 into the gain control path so that signals below the threshold can not affect the gain of the receiver.

18. Remote Manual Gain

Remote manual gain is controlled via the DAC, U21. U12b and U11c are open and U11d is closed, allowing the DAC to set up a voltage threshold, similar to that produced in the manual gain mode.

Strong Signals Outside Filter Bandwidth

19. Additional inputs are available to U17d from the R143/R144 network. this network becomes effective when strong signals are present within the 16kHz bandwidth of the roofing filter, but outside the bandwidth of the selected filter. Since the AGC is derived from circuitry after the selectable filters, it is possible that the receiver front-end could become overloaded with its gain kept at a high level, due to failure of the AGC to act on a strong signal outside the bandwidth of the selected filter.

Diversity AGC

20. Diversity AGC is possible by connecting the diversity lines of two receivers. When either RA1792 receives a strong signal its diversity line goes low, pulling down the voltage on U14b pin 13 on the other receiver, forcing U14b output to go high and thus reducing receiver gain via CR19 and U14a.

ISB Gain Control

21. When the ISB option is being used, the input of the integrator on the ISB board is applied to U17c pin 9. U19c output, pin 8, is applied to the A 757 on the ISB board and also to CR27. In the ISB mode, CR26 passes the USB signal and CR27 passes the LSB signal. The junction of CR26 and CR27 is a virtual earth point, allowing the highest signal level through either diode to control the gain of the first IF amplifier through U17d. In this mode the second IF amplifier operates independently.

## DEMODULATION AND AF

22. The output from the AGC controlled IF amplifier is filtered by L1, L2 and associated components and then buffered by Q6, an emitter follower. The signal is then passed to the RF switch.

### RF Switch

23. The RF Switch comprises CR22 to CR25 and associated components. The BFO signal, when sideband operation is selected, enters on J5, is immediately available on J6, and is switched by the CR22 and CR24 circuit. Normal IF, either AM or FM, is switched by the CR23 and CR25 circuit. Control is applied from U4 $\overline{Q2}$ and U4 Q2 so that one signal path through the RF switch is always selected. The signal thus selected, either BFO or IF, is applied to the input port of U18, the Limiting Amplifier and FM detector.

### FM and AM Detectors

24. When the signal applied to U18 is Frequency Modulated, an AF output will be available at pin 1 and this is passed directly to U19a which is the detector select switch. Pin 10 is the carrier port of the FM detector, U18, and a carrier is always available at approximately 1.2v p.p from this port. Signals which are not FM are passed from U18 pin 10, RF output, to the carrier port of U20 which is an AM product detector. At the same time the unchanged IF signal from Q6 is applied to U20 pin 1, the signal input. The AF output from U20 pin 6 is taken to the detector select switch U19a. This switch is controlled by the microcomputer via one of four latches in U23.

### Audio Low Pass Filter

25. The AF output selected by U19a is passed through a low-pass filter comprising U28 and its components. The 3dB point of this filter occurs at approximately 5kHz. The gain of the filter may be set at unity by operation of U19b which is controlled by the microcomputer via one of four latches in U23.

### Audio Crosspoint Switch

26. U25 is an Audio Crosspoint Switch having four inputs, X1 - X4, and four outputs, Y1 - Y4. Any input may be switched to any output and any number of these connections may be made simultaneously. U25 has internal latches which allow switching information to be retained until it is changed by the microcomputer, or until power is removed from the system. The inputs and outputs are as follows:

X1 : AF Input from Audio Low Pass Filter
X2 : AF Input from ISB (when fitted)
X3 : External line 2 input from A4J8 pin 32, or from U29b which is used as a line buffer.
X4 : External line 1 input from A4J8 pin 30, or from U29a which is used as a line buffer.

Y1 : AF output via line level control R129 to input of U29a
Y2 : AF output via line level control R132 to input of U29b

Y3 : AF output to phones and line amplifier
Y4 : AF output via front panel volume control, to loudspeaker amplifier. Also to U19c for later AF level measurement.

AF Output Amplifiers

27. U26 consists of two audio amplifiers in a single package. The first of these has a gain of approximately 5, amplifying the signal from U25 pin 10 (Y3 output) before application to T1. T1 provides a monitor line output to A4J7 pins 7 & 8 with ground or centre tap available on pin 9, depending upon type of transformer fitted. A4J7 pin 11 is permanently connected to 0V.

28. The second amplifier in the U26 package is the loudspeaker amplifier and is driven from U25 pin 11, (Y4 output) via the front panel volume control. The AF output is available on A4J2 pin 10 and A4J7 pin 10.

AF AND RF LEVEL MEASUREMENTS

AF Levels

29. AF level measurements are made from one of two different points : For normal front panel display the reading is taken from after the line level potentiometers (R129, R132) whilst readings for BITE (Built in Test Equipment) are taken from a point before the line level preset controls. U19c is used to switch the chosen signal to U22a which detects the peak of the AF signal and applies this to U24a, pin 8.

RF Levels

30. The main RF level is measured as a function of the AGC voltage level, which is applied to U24c. The diversity AGC line is also connected to this point from A4J7 pin 16. When a second receiver is used in diversity mode, the strongest RF level available from either of the receivers is measured. When the ISB option is fitted, ISB AGC voltage is applied to U24b for measurement in a similar manner to the main RF level for both normal and diversity working.

Measurement

31. This is achieved by a fast method of successive approximation. The Digital to Analogue converter U21 is connected to the inverting inputs of voltage comparators U24a, U24b and U24c. The voltage to be measured is applied to the inverting input : AF on U24a; ISB on U24b and Main RF on U24c. U21 is first required to provide an output of 5 volts, half its total range of 10V, and the output of the comparator in use is sampled by the microprocessor. If the comparator's output is low then the next voltage supplied from the D-A converter will be half way between full voltage and the previous output, i.e. 7.5 V. If the comparator's output is high then the next D-A voltage will be between 0V and the previous output, i.e. 2.5 V.

This continues with the intervals becoming progressively smaller until the point is reached where the output toggles between two adjacent voltages and the high state is accepted by the microprocessor as the correct reading. The D-A byte which produced this state is then stored and the voltage reading is completed, with the stored byte representing the voltage which has been measured.

BITE

32. BITE (Built in Test Equipment) measures the AF, ISB and Main RF signal levels by means of the Digital to Analogue converter, U21, when the automatic test sequence is entered by means of the receiver front panel controls. AF measurements are made from a point independent of level controls.

33. U24d on the Main IF/AF module is used by BITE, the D-A converter output voltage being applied to the non-inverting input and voltages to be measured being applied to the other input from the BITE multiplexer, situated on the Front Panel Memory Board, A9A2. Voltages to be measured enter the IF/AF module via A4J2 pin 7, and the comparator output is available from A4J2 pin 5.

## MAIN IF/AF BOARD A4 (ST 82914)

| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R1 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R2 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R3 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R4 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R5 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R6 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R7 | 15k | Metal Oxide | ¼ | ±2 | 920645 |
| R8 | 47 | Metal Oxide | ¼ | ±2 | 917063 |
| R9 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R10 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R11 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R12 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R13 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R14 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R15 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R16 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R17 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R18 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R19 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R20 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R21 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R22 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R23 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R24 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R25 | 100 | Metal Oxide | ¼ | ±2 | 910388 |
| R26 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R27 | 1.5k | Metal Oxide | ¼ | ±2 | 911166 |
| R28 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R29 | 47 | Metal Oxide | ¼ | ±2 | 917063 |
| R30 | 22k | Metal Oxide | ¼ | ±2 | 913493 |

| Cct. Ref. | Value | Description | Rat. | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R31 | 3.3k | Metal Oxide | ¼ | ±2 | 910111 |
| R32 | 47k | Metal Oxide | ¼ | ±2 | 913496 |
| R33 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R34 | 2.7k | Metal Oxide | ¼ | ±2 | 916548 |
| R35 | 560 | Metal Oxide | ¼ | ±2 | 917061 |
| R36 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R37 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R38 | 47k | Metal Oxide | ¼ | ±2 | 913496 |
| R39 | 2k | Variable | | | 941939 |
| R40 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R41 | 47k | Metal Oxide | ¼ | ±2 | 913496 |
| R42 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R43 | 680 | Metal Oxide | ¼ | ±2 | 910113 |
| R44 | 1.5k | Metal Oxide | ¼ | ±2 | 911166 |
| R45 | 220k | Metal Oxide | ¼ | ±2 | 921771 |
| R46 | 47 | Metal Oxide | ¼ | ±2 | 917063 |
| R47 | 50k | Variable | | 20 | 941941 |
| R48 | 680 | Metal Oxide | ¼ | ±2 | 910113 |
| R49 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R50 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R51 | 2.2k | Metal Oxide | ¼ | ±2 | 916546 |
| R52 | 47k | Metal Oxide | ¼ | ±2 | 913496 |
| R53 | 33k | Metal Oxide | ¼ | ±2 | 913495 |
| R54 | 220k | Metal Oxide | ¼ | ±2 | 921771 |
| R55 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R56 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R57 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R58 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R59 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R60 | 100 | Metal Oxide | ¼ | ±2 | 910388 |
| R61 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R62 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R63 | 1.5k | Metal Oxide | ¼ | ±2 | 911166 |
| R64 | 1.5k | Metal Oxide | ¼ | ±2 | 911166 |
| R65 | 15k | Metal Oxide | ¼ | ±2 | 920645 |

| Cct. Ref. | Value | Description | Rat. | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R66 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R67 | 18k | Metal Oxide | ¼ | ±2 | 900994 |
| R68 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R69 | 15k | Metal Oxide | ¼ | ±2 | 920645 |
| R70 | 1.2k | Metal Oxide | ¼ | ±2 | 911179 |
| R71 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R72 | 1k | Metal Ocide | ¼ | ±2 | 913489 |
| R73 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R74 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R75 | 390 | Metal Oxide | ¼ | ±2 | 916331 |
| R76 | 3.3k | Metal Oxide | ¼ | ±2 | 910111 |
| R77 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R78 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R79 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R80 | 47 | Metal Oxide | ¼ | ±2 | 917063 |
| R81 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R82 | 39 | Metal Oxide | ¼ | ±2 | 917062 |
| R83 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R84 | 3.3k | Metal Oxide | ¼ | ±2 | 910111 |
| R85 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R86 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R87 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R88 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R89 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R90 | 47k | Metal Oxide | ¼ | ±2 | 913496 |
| R91 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R92 | 3.9k | Metal Oxide | ¼ | ±2 | 915074 |
| R93 | 47k | Metal Oxide | ¼ | ±2 | 913496 |
| R94 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R95 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R96 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R97 | 18k | Metal Oxide | ¼ | ±2 | 900994 |
| R98 | 12k | Metal Oxide | ¼ | ±2 | 917952 |
| R99 | 27k | Metal Oxide | ¼ | ±2 | 913494 |
| R100 | 10 | Metal Oxide | ¼ | ±2 | 920736 |

| Cct. Ref. | Value | Description | Rat. | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R101 | 2.2k | Metal Oxide | ¼ | ±2 | 916546 |
| R102 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R103 | 47k | Metal Oxide | ¼ | ±2 | 913496 |
| R104 | 18k | Metal Oxide | ¼ | ±2 | 900994 |
| R105 | 10k | Variable | | | 941940 |
| R106 | 180k | Metal Oxide | ¼ | ±2 | 920644 |
| R107 | 18k | Metal Oxide | ¼ | ±2 | 900994 |
| R108 | 6.8k | Metal Oxide | ¼ | ±2 | 910112 |
| R109 | 3.3k | Metal Oxide | ¼ | ±2 | 910111 |
| R110 | 470 | Metal Oxide | ¼ | ±2 | 920758 |
| R111 | 3.3k | Metal Oxide | ¼ | ±2 | 910111 |
| R112 | 3.3k | Metal Oxide | ¼ | ±2 | 910111 |
| R113 | 1.5k | Metal Oxide | ¼ | ±2 | 911166 |
| R114 | 3.3k | Metal Oxide | ¼ | ±2 | 910111 |
| R115 | 47 | Metal Oxide | ¼ | ±2 | 917063 |
| R116 | 3.3k | Metal Oxide | ¼ | ±2 | 910111 |
| R117 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R118 | 10k | Metal Oxide | ¼ | ±2 | 914042 |
| R119 | 10k | Variable | | 20 | 941940 |
| R120 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R121 | 1.8k | Metal Oxide | ¼ | ±2 | 911148 |
| R122 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R123 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R124 | 22k | Metal Oxide | ¼ | ±2 | 913493 |
| R125 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R126 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R127 | 8.2k | Metal Oxide | ¼ | ±2 | 918202 |
| R128 | 2.2k | Metal Oxide | ¼ | ±2 | 916546 |
| R129 | 2k | Variable | | 20 | 938453 |
| R130 | 22 | Metal Oxide | ¼ | ±2 | 920743 |
| R131 | 22 | Metal Oxide | ¼ | ±2 | 920743 |
| R132 | 2k | Variable | | 20 | 938453 |
| R133 | 10 | Metal Oxide | ¼ | ±2 | 920736 |
| R134 | 27k | Metal Oxide | ¼ | ±2 | 913494 |
| R135 | 10k | Metal Oxide | ¼ | ±2 | 914042 |

| Cct. Ref. | Value | Description | Rat. | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R136 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R137 | 4.7k | Metal Oxide | ¼ | ±2 | 913490 |
| R138 | 100 | Metal Oxide | ¼ | ±2 | 910388 |
| R139 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R140 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R141 | 100 | Metal Oxide | ¼ | ±2 | 910388 |
| R142 | 33 | Metal Oxide | ¼ | ±2 | 917060 |
| R143 | 1.5k | Metal Oxide | ¼ | ±2 | 911166 |
| R144 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R145 | 1k | Metal Oxide | ¼ | ±2 | 913489 |
| R146 | | Not Used | | | |
| R147 | | Not Used | | | |
| R148 | | Not Used | | | |
| R149 | | Not Used | | | |
| R150 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R151 | 100k | Metal Oxide | ¼ | ±2 | 915190 |
| R152 | 1k | Metal Oxide | | ±2 | 913489 |
| R153 | 270k | Metal Oxide | | ±2 | 923598 |
| R154 | 1k | Metal Oxide | | ±2 | 913489 |
| **Capacitors** | | | | | |
| | µF | | | | |
| C1 to C12 | | Part of filter assemblies FL1 to FL6 | | | |
| C13 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C14 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C15 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C16 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C17 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C18 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C19 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C20 | 15 | Tantalum | 20 | ±20 | 938034 |
| C21 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C22 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C23 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C24 | 0.1 | Ceramic | 50 | ±20 | 928406 |
| C25 | 0.1 | Ceramic | 50 | ±20 | 938406 |

| Cct. Ref. | Value µF | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| Capacitors | | | V | | |
| C26 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C27 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C28 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C29 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C30 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C31 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C32 | 15 | Tantalum | 20 | ±20 | 938034 |
| C33 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C34 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C35 | 68 | Tantalum | 25 | ±10 | 931176 |
| C36 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C37 | 1000p | Ceramic | | 20 | 938408 |
| C38 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C39 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C40 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C41 | 0.022 | Ceramic | | ±20 | 930219 |
| C42 | 6.8 | Tantalum | 35 | ±20 | 938030 |
| C43 | 0.01 | Ceramic | | ±20 | 938053 |
| C44 | 1500p | Silver Mica | | ±1 | 943146 |
| C45 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C46 | 82p | Silver Mica | | ±2 | 902232 |
| C47 | 1500p | Silver Mica | | ±1 | 943146 |
| C48 | 1000p | Ceramic | | 20 | 938408 |
| C49 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C50 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C51 | 0.01 | Ceramic | | ±20 | 938053 |
| C52 | 15 | Tantalum | 20 | ±20 | 938034 |
| C53 | 0.01 | Ceramic | | ±20 | 938053 |
| C54 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C55 | | Not Used | | | |
| C56 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C57 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C58 | 15 | Tantalum | 20 | ±20 | 938034 |
| C59 | 6.8 | Tantalum | 35 | ±20 | 938030 |
| C60 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C61 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C62 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C63 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C64 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C65 | 0.1 | Ceramic | 50 | ±20 | 938406 |

| Cct. Ref. | Value µF | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| Capacitors | | | V | | |
| C66 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C67 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C68 | 3300p | Silver Mica | 500 | ±2 | 943147 |
| C69 | 0.01 | Ceramic | 50 | ±20 | 938053 |
| C70 | 0.1 | Ceramic | 50 | ±10 | 940318 |
| C71 | 100p | Silver Mica | 350 | ±2 | 902234 |
| C72 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C73 | 100 | Electrolytic | 25 | +50 -10 | 921546 |
| C74 | 1 | Ceramic | 50 | ±20 | 938401 |
| C75 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C76 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C77 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C78 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C79 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C80 | 15 | Tantalum | 20 | ±20 | 938034 |
| C81 | 0.1 | Ceramic | 50 | ±10 | 940318 |
| C82 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C83 | 3.3 | Tantalum | 35 | ±20 | 933933 |
| C84 | 10p | Ceramic | 500 | ±.5p | 938446 |
| C85 | 6.8 | Tantalum | 35 | ±20 | 938030 |
| C86 | 1 | Tantalum | 35 | 20 | 938405 |
| C87 | 1 | Tantalum | 35 | 20 | 938405 |
| C88 | 4700p | Ceramic | 100 | ±5 | 938437 |
| C89 | 2200p | Ceramic | 100 | ±5 | 938438 |
| C90 | 220 | Electrolytic | 16 | +50 -10 | 938436 |
| C91 | 6.8 | Tantalum | 35 | ±20 | 938030 |
| C92 | 470 | Electrolytic | 25 | +100 -10 | 938439 |
| C93 | 15 | Tantalum | 20 | ±20 | 938034 |
| C94 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C95 | 6.8 | Tantalum | 35 | ±20 | 938030 |
| C96 | 6.8 | Tantalum | 35 | ±20 | 938030 |
| C97 | 6.8 | Tantalum | 35 | ±20 | 938030 |
| C98 | 6.8 | Tantalum | 35 | ±20 | 938030 |
| C99 | 220 | Electrolytic | 16 | +50 -10 | 938436 |
| C100 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C101 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C102 | 15 | Tantalum | 20 | ±20 | 938034 |
| C103 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C104 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C105 | 220 | Electrolytic | 16 | +50 -10 | 938436 |

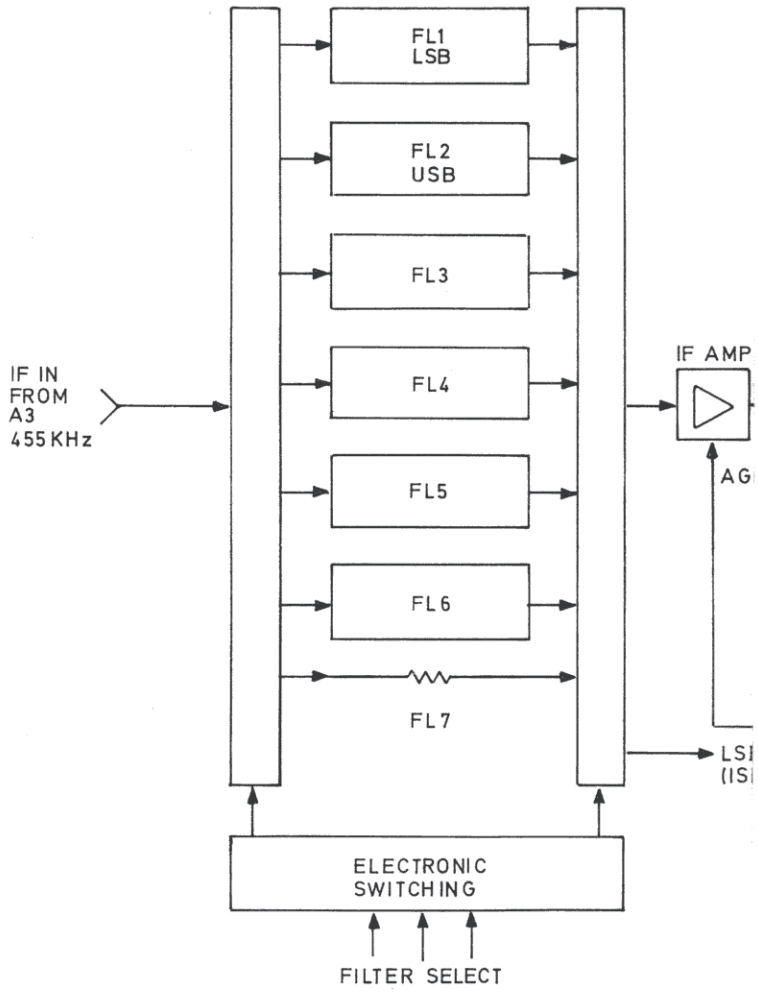
| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| **Capacitors** | µF | | V | | |
| C106 | 6.8 | Tantalum | 50 | ±20 | 943427 |
| C107 | 68 | Tantalum | 15 | ±20 | 938036 |
| C108 | 220 | Electrolytic | 16 | +50 -10 | 938436 |
| C109 | ) | Part of Filter Assembly | | | |
| C110 | ) | FL7 | | | |
| C111 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C112 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C113 | 15 | Tantalum | 20 | ±20 | 938034 |
| C114 | | Not Used | | | |
| C115 | | Not Used | | | |
| C116 | | Not Used | | | |
| C117 | | Not Used | | | |
| C118 | | Not Used | | | |
| C119 | | Not Used | | | |
| C120 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| C121 | 0.1 | Ceramic | 50 | ±20 | 938406 |
| **Diodes** | | | | | |
| CR1 | | IN916 | | | 913480 |
| CR2 | | IN916 | | | 913480 |
| CR3 | | IN916 | | | 913480 |
| CR4 | | IN916 | | | 913480 |
| CR5 | | 1N916 | | | 913480 |
| CR6 | | IN916 | | | 913480 |
| CR7 | | IN916 | | | 913480 |
| CR8 | | IN916 | | | 913480 |
| CR9 | | IN916 | | | 913480 |
| CR10 | | IN916 | | | 913480 |
| CR11 | | IN916 | | | 913480 |
| CR12 | | IN916 | | | 913480 |
| CR13 | | IN916 | | | 913480 |
| CR14 | | IN916 | | | 913480 |
| CR15 | | IN916 | | | 913480 |
| CR16 | | IN916 | | | 913480 |
| CR17 | | IN916 | | | 913480 |
| CR18 | | IN916 | | | 913480 |
| CR19 | | IN916 | | | 913480 |
| CR20 | | IN916 | | | 913480 |

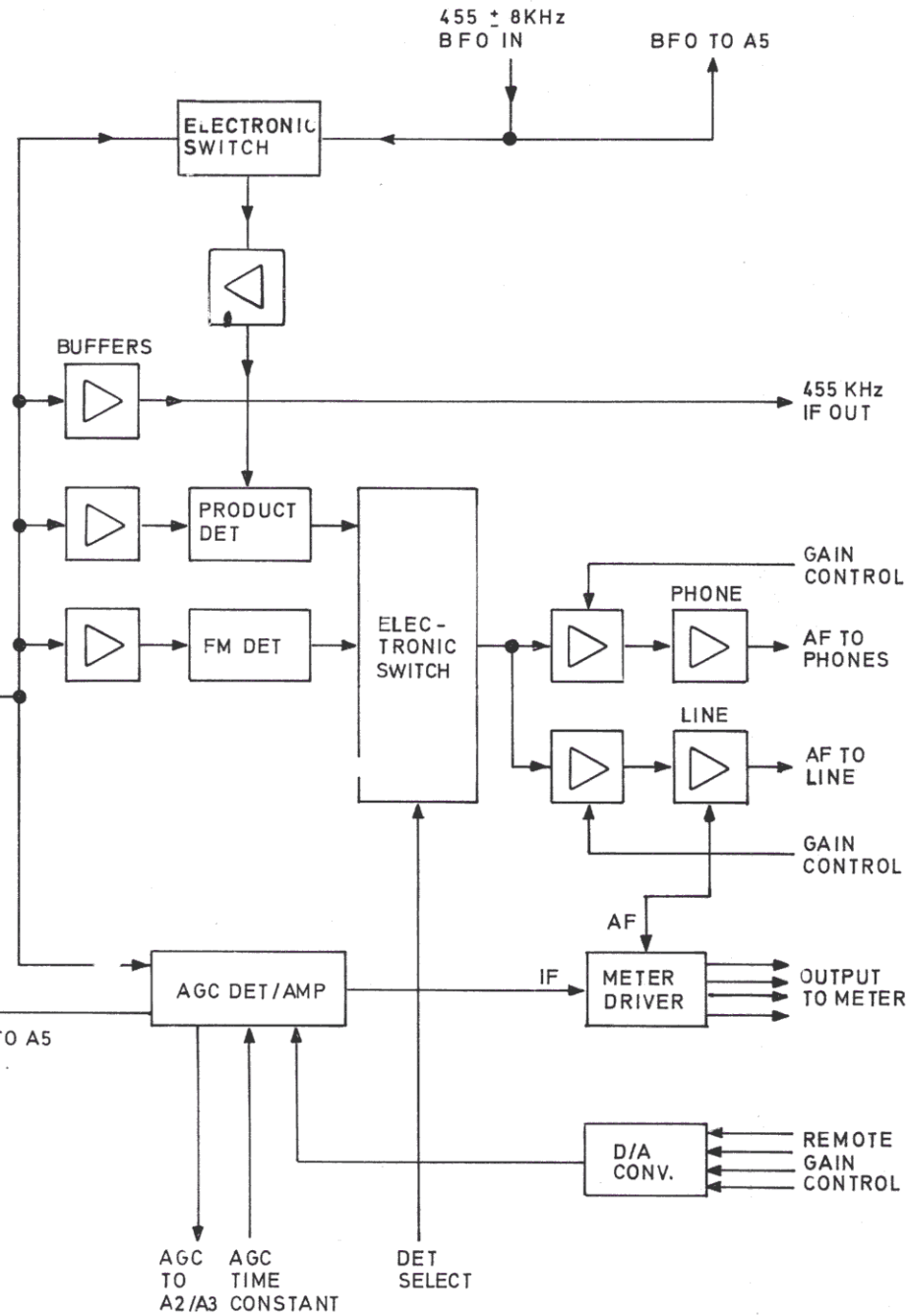
| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| **Diodes** | | | | | |
| CR21 | | IN916 | | | 913480 |
| CR22 | | IN916 | | | 913480 |
| CR23 | | IN916 | | | 913480 |
| CR24 | | IN916 | | | 913480 |
| CR25 | | IN916 | | | 913480 |
| CR26 | | IN916 | | | 913480 |
| CR27 | | IN916 | | | 913480 |
| CR28 | | IN916 | | | 913480 |
| CR29 | | IN916 | | | 913480 |
| CR30 | | IN916 | | | 913480 |
| CR31 | | IN916 | | | 913480 |
| **Transistors** | | | | | |
| Q1 | | Silicon (2N5089) | | | 938417 |
| Q2 | | Silicon (2N5089) | | | 938417 |
| Q3 | | Silicon (2N5089) | | | 938417 |
| Q4 | | Silicon (T1 S74) | | | 938450 |
| Q5 | | Silicon (2N3906) | | | 914047 |
| Q6 | | Silicon (2N5089) | | | 938417 |
| Q7 | | Silicon (2N5089) | | | 938417 |
| Q8 | | Silicon (2N5089) | | | 938417 |
| Q9 | | Silicon (2N5089) | | | 938417 |
| Q10 | | Not Fitted | | | |
| Q11 | | Not Fitted | | | |
| **Integrated Circuits** | | | | | |
| U1 | | 4028 | | | 929707 |
| U2 | | 4042 | | | 930861 |
| U3 | | 40109 | | | 931054 |
| U4 | | 4042 | | | 930861 |
| U5 | | 40109 | | | 931054 |
| U6 | | 78L12 | | | 938455 |
| U7 | | 324 | | | 925944 |
| U8 | | 757 | | | 921201 |
| U9 | | 4013 | | | 933644 |
| U10 | | CA3046 | | | 922907 |

| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| **Integrated Circuits** | | | | | |
| U11 | | 4066 | | | 930148 |
| U12 | | 4066 | | | 930148 |
| U13 | | 4042 | | | 930861 |
| U14 | | 324 | | | 925944 |
| U15 | | 4042 | | | 930861 |
| U16 | | 40109 | | | 931054 |
| U17 | | 324 | | | 925944 |
| U18 | | ULN2111A | | | 943835 |
| U19 | | 4053 | | | 938457 |
| U20 | | MC1496P | | | 938427 |
| U21 | | AD7524 | | | 938458 |
| U22 | | 1458 | | | 938459 |
| U23 | | 4042 | | | 930861 |
| U24 | | 339 | | | 929149 |
| U25 | | CD22100 | | | 938460 |
| U26 | | LM377N | | | 938753 |
| U27 | | 7812 | | | 938445 |
| U28 | | 1458 | | | 938459 |
| U29 | | 1458 | | | 938459 |
| U30 | | Not Fitted | | | |
| U31 | | Not Fitted | | | |
| **Transformers** | | | | | |
| T1 | | | | | AT81401 |
| **Inductors** | | | | | |
| L1 | | RF Coil | | | AT81400 |
| L2 | | RF Coil | | | AT81400 |
| L3 | | RF Coil | | | AT81408 |
| L4 | 10µH | Choke | | | 921209 |
| **Connectors** | | | | | |
| J1 | | Plug, Coaxial RF | | | 938429 |
| J2 | | Plug, 40-way | | | 928475 |
| J3 | | Plug, Coaxial RF | | | 938429 |
| J4 | | Plug, Coaxial RF | | | 938429 |
| J5 | | Plug, Coaxial RF | | | 938429 |
| J6 | | Plug, Coaxial RF | | | 938429 |
| J7 | | Plug, 26-way | | | 928473 |
| J8 | | Plug, 34-way | | | 927062 |

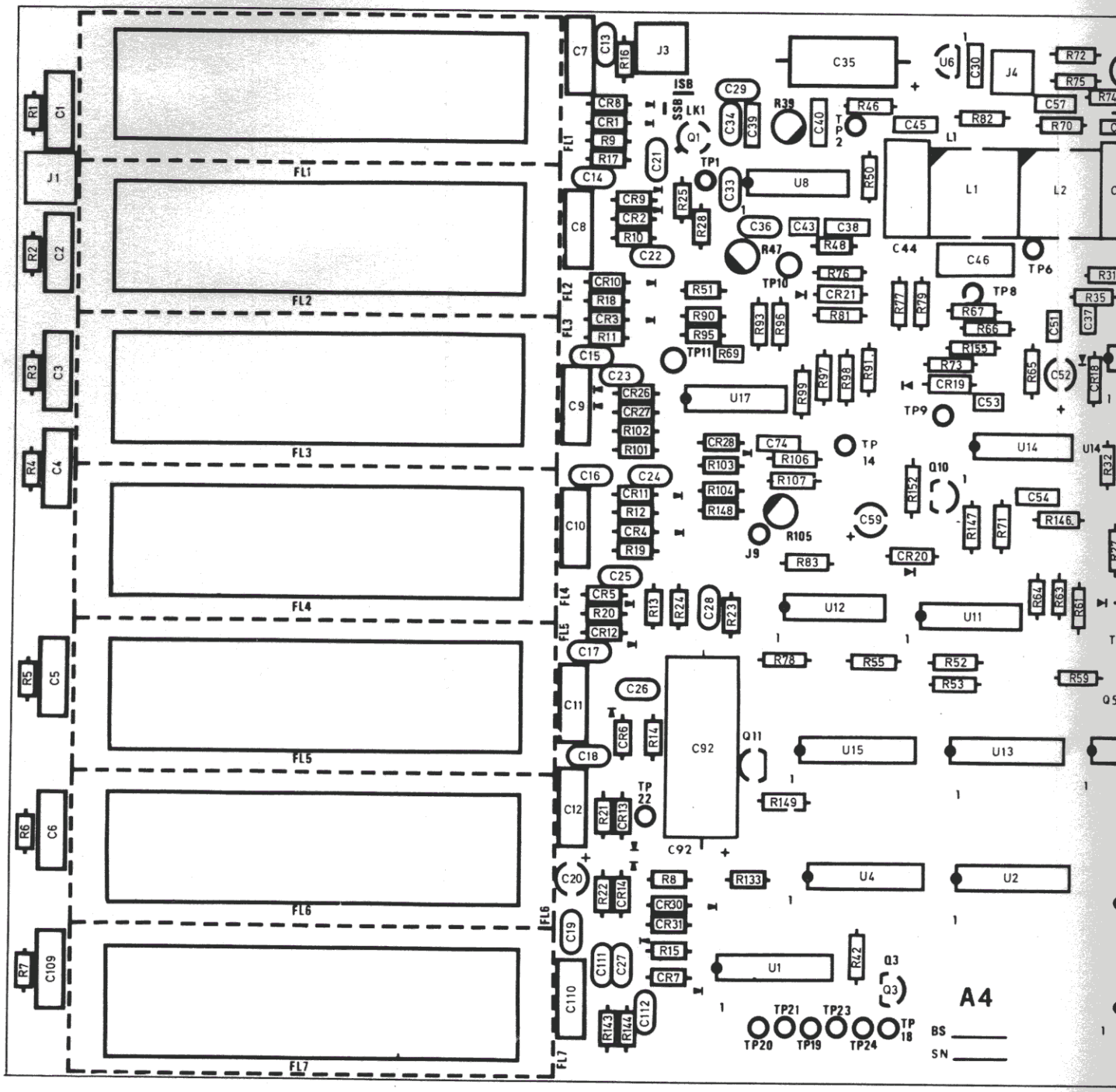
| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| Filters | | Sideband: | | | |
| | | 0.34 kHz SSB | | | BD81062 |
| | | 0.4 kHz SSB | | | BD81068 |
| | | 0.8 kHz SSB | | | BD81063 |
| | | *2.7 kHz USB Marine | | | BD81052 |
| | | 2.7 kHz LSB | | | BD81084 |
| | | 2.7 kHz USB | | | BD81085 |
| | | *3.0 kHz LSB | | | BD81058 |
| | | 3.0 kHz LSB | | | BD81081 |
| | | *3.0 kHz USB | | | BD81059 |
| | | 3.0 kHz USB | | | BD81082 |
| | | 6.0 kHz LSB | | | BD82791 |
| | | 6.0 kHz USB | | | BD82793 |
| | | Symmetrical | | | |
| | | *0.1 kHz | | | BD81023 |
| | | 0.15 kHz | | | BD81067 |
| | | *0.3 kHz | | | BD81053 |
| | | 0.3 kHz | | | BD81078 |
| | | *1.0 kHz | | | BD81054 |
| | | 1.0 kHz | | | BD81079 |
| | | *1.6 kHz | | | BD81015 |
| | | *2.0 kHz | | | BD81016 |
| | | 2.5 kHz | | | BD81065 |
| | | *3.2 kHz | | | BD81055 |
| | | 3.2 kHz | | | BD81083 |
| | | 4.0 kHz | | | BD81064 |
| | | 5.0 kHz | | | BD81066 |
| | | *6.0 kHz | | | BD81056 |
| | | 6.0 kHz | | | BD81080 |
| | | *16.0 kHz | | | BD81057 |

* These are mechanical filters


FL1
LSB
FL2
USB
FL3
FL4
FL5
FL6
FL7
IF IN
FROM
A3
455 KHz
IF AMP
AG
LSI
(ISI
ELECTRONIC
SWITCHING
FILTER SELECT



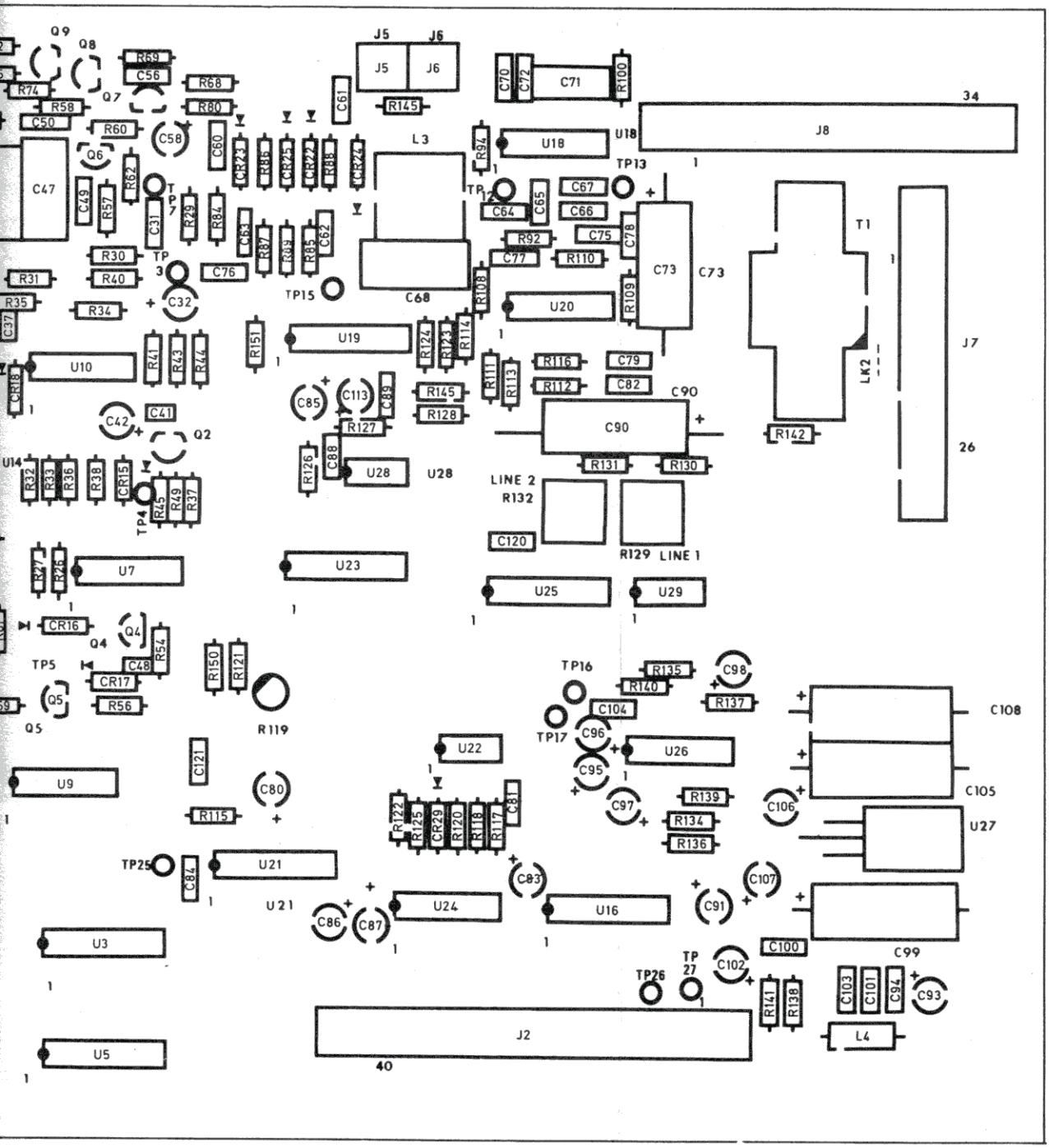

Simplified Block Diagram Fig.5.1
Main IF/AF A4




EA 82913 /4 155 RA 1792

IDENT

MAIN IF\AF BOARD (A4)




EA82913 / 4 [5]

Component Layout
Main IF/AF Board Fig.5.3

# CHAPTER 5

## MAIN IF/AF MODULE A4 (ST 82914)

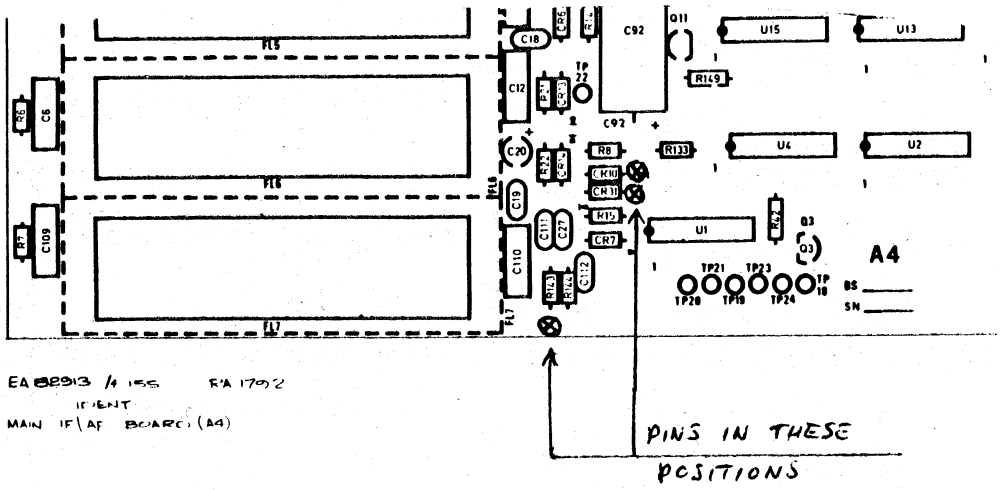
## ADDENDUM

The following change effects Option KA/S2/S/D/5/A only and any RA1792's having a filter fitted in position FL7. This change is to help to eliminate stray coupling.

1. Remove and discard from Main IF/AF Board:

| | | |
|---|---|---|
| R143(1K5) | C111(0µ1) | CR30(1N916) |
| R144(1K0) | C112(0µ1) | CR31(1N916) |

2. Fit Oxley pins (943646) at points marked ⊠ on Fig 5.3 (as shown below) allowing 5mm protrusion on underside of board.




RACAL

| TH 1496 | EA82913 |
|---|---|
| 5 | |

3. Fit new pin board utilising fixing studs and nuts of Filters 5 and 6 (using plain washers as spacers between boards).

4. Fit the following items to board and connect flying leads as shown in sketch overleaf.

# CHAPTER 7

# FIRST L.O. SYNTHESIZER A7

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| 2 | FUNCTIONAL DESCRIPTION | 7-2 |
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| 8 | Divide-by-four Stage | 7-4 |
| 9 | 9.1V C-MOS Supply | 7-4 |
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| 14 | D-A Converter | 7-5 |
| 15 | Phase Comparator | 7-6 |
| 21 | Division Ratio to Voltage Converter | 7-8 |
| 22 | Fast Lock Detector | 7-8 |
| 24 | 40.455 MHz to 70.455 MHz VCO | 7-9 |
| | Components List | |


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| 7-2 | Block Diagram : Synthesizer Board | 7-3 |
| 7-3 | Timing Diagram : Presettable Binary Counter | 7-6 |
| 7-4 | Timing Diagram : Divider Frequency High | 7-7 |
| 7-5 | Timing Diagram : Divider Frequency Low | 7-7 |
| 7-6 | Timing Diagram : Divider & Reference in Phase | 7-8 |
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| 7-8 | Circuit: Alternative Prescaler MC12012 | |
| 7-9 | Component Layout : First L.O. Synthesizer | |

# CHAPTER 7

# FIRST L.O. SYNTHESIZER A7

## INTRODUCTION

1. A single-loop synthesizer is used to produce the 40.605 MHz to 70.455 MHz local oscillator signal, which is applied to the mixer board. It makes use of an LSI device (U9) which contains the synthesizer control circuitry. A simplified block diagram of this device is given in fig.7.1.

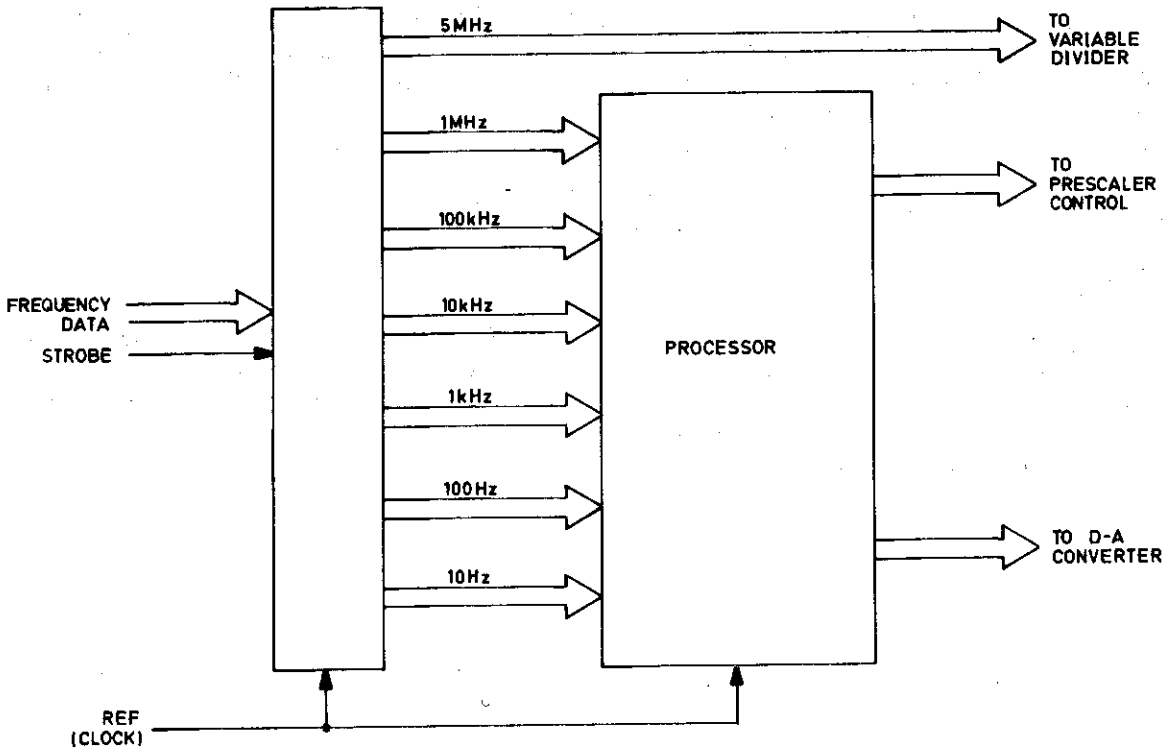



Fig. 7-1 BLOCK DIAGRAM : SYNTHESIZER CONTROL DEVICE, U9

## FUNCTIONAL DESCRIPTION

2. The block diagram of the synthesizer board given in fig. 7-2. An output signal from the 40.605 MHz to 70.455 MHz VCO (Q8) is applied to a phase comparator via a buffer amplifier Q1, Q2, Q3, a shaper stage U4 and a programmed divider comprising a divide-by-5/divide-by-6 prescaler U6 and a variable divider U11 (both controlled by U9) together with output buffer and reclocking stages U14a, U14b. A 1 MHz reference signal from the control stage is first re-synchronised to a 5 MHz signal derived from the 20 MHz reference signal, and is then applied as the second input to the phase comparator. The main output signal from the phase comparator is then applied to a pulse-width integrator (U19a) to produce the varactor control voltage which is applied to the VCO via a summing node, a further integrator (U21), and the loop amplifier U19b.

3. Thus the phase comparator output signal drives the VCO until its frequency, when divided by the programmed divider, is equal to the 1 MHz reference frequency, and phase-lock is then achieved.

4. The division ratio to voltage conversion stage is fed from the $\overline{Q}$ output of the re-clocking stage U14, and produces an output voltage which is proportional to the programmed divider division ratio. This circuit is included to increase the effective phase comparator gain with an increasing division ratio and so maintain a constant loop bandwidth.

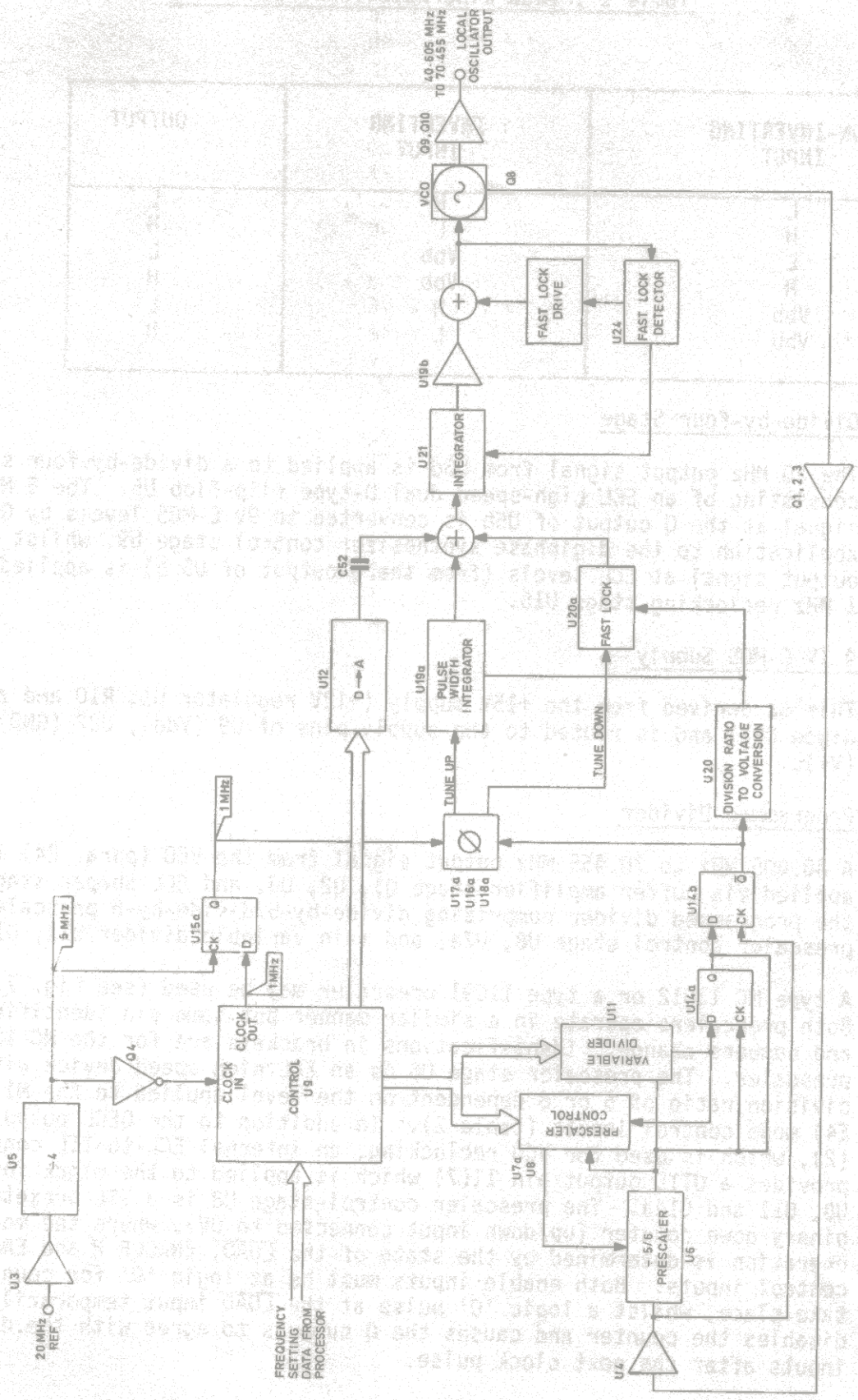
5. The fast lock circuit provides additional control only when the loop is out of lock. The output is summed with that from the pulse-width integrator and also that from a digital-to-analogue converter with differentiating capacitor C52. This latter stage is included to control the phase of the loop current and further reduce spurious levels.

6. The output signal from integrator stage U21 is applied via loop amplifier U19b to the varactor diodes of the VCO, and is also applied to a fast lock detector. This stage is used to detect a change in the receiver frequency setting and then rapidly drives the VCO, either up or down, as necessary, to bring about a rapid return to the locked condition.

## CIRCUIT DESCRIPTION (figs. 7-7 and 7-8)

### Reference Input Shaper

7. The 20 MHz reference signal at A7J2 is coupled by C14 to a wideband amplifier/limiter stage which uses all four sections of a quad line receiver device U3. This is an ECL (emitter coupled logic) device and contains a Vbb supply generator which is used to set the input and output threshold levels (table 1).




RA1792 Fig. 7-2 BLOCK DIAGRAM : SYNTHESIZER BOARD 7-3

Table 1 : Quad Line Receiver Truth Table

| NON-INVERTING INPUT | INVERTING INPUT | OUTPUT |
|---|---|---|
| L | H | L |
| H | L | H |
| L | Vbb | L |
| H | Vbb | H |
| Vbb | H | L |
| Vbb | L | H |

Divide-by-four Stage

8. The 20 MHz output signal from U3d is applied to a divide-by-four stage consisting of an ECL high-speed dual D-type flip-flop U5. The 5 MHz signal at the Q output of U5b is converted to 9V C-MOS levels by Q4 before application to the digiphase synthesizer control stage U9, whilst a 5 MHz output signal at ECL levels (from the $\overline{Q}$ output of U5 b) is applied to the 1 MHz reclocking stage U15.

9.1V C-MOS Supply

9. This is derived from the +15V supply (+12V regulator U1, R10 and zener diode CR1) and is routed to the supply pins of U9 (Vdd), U22 (GND) and U12 (V+).

Programmed Divider

10. A 40.605 MHz to 70.455 MHz output signal from the VCO (para. 24) is applied via buffer amplifier stage Q1, Q2, Q3, and ECL shaper stage U4, to the programmed divider comprising divide-by-5/divide-by-6 prescaler U6, prescaler control stage U8, U7a, and main variable divider U11, U14a.

11. A type MC 12012 or a type 11C91 prescaler may be used (see Fig. 7.8). Both prescalers operate in a similar manner but some pin identifications and numbers change. Identifications in brackets are for the MC 12012 prescaler. The prescaler stage U6 is an ECL high speed device with a division ratio of 5 or 6 dependent on the level applied to the M1, M2 (E3, E4) mode control inputs (table 2). In addition to the QECL output pin 8 (2), which is used for VCO reclocking, an internal ECL-to-TTL converter provides a QTTL output pin 11(7) which is applied to the clock inputs of U8, U11 and U14a. The prescaler control stage U8 is a TTL presettable binary down counter (up/down input connected to 0V), where the mode of operation is determined by the state of the $\overline{\text{LOAD}}$, ENABLE $\overline{P}$ and ENABLE $\overline{T}$ control inputs. Both enable inputs must be at logic '0' for counting to take place, whilst a logic '0' pulse at the $\overline{\text{LOAD}}$ input temporarily disables the counter and causes the Q outputs to agree with the data inputs after the next clock pulse.

Table 2 : Prescaler Mode Control

| INPUTS | | OUTPUT RESPONSE |
|---|---|---|
| M1 (E3) | M2 (E4) | |
| L | L | ÷6 |
| X | H | ÷5 |
| H | X | ÷5 |

12. U8 thus counts down from the preset number at the A, B, C and D input pins, and whilst this counting-down is in progress, because at least one of the QB, QC or QD outputs will be at logic '1', the output from NOR gate U7a is maintained at a '0', U8 is enabled, and U6 divides by 6. When U8 counts down to numeral 1 i.e. QB, QC and QD outputs all at '0', the output from U7a changes to a '1', U8 is disabled, and U6' divides by 5. This condition is maintained until the application of the next preset-enable (LOAD) pulse from U11, at which time the cycle is repeated.

13. The main programmed divider stage U11 is also a TTL presettable binary down counter (up/down input connected to OV), which is permanently enabled by connecting both enable inputs to OV. It counts down from the preset number at the A, B, C and D input pins, and produces a negative-going pulse at the ripple-carry output (RCO) pin each time a count of zero is reached (fig. 7-3). This output is applied via buffer stage U14a to the VCO reclocking stage U14b, and also to the $\overline{\text{LOAD}}$ input pins of U8 and U11 to preset-enable both counters.

D-A Converter

14. U12 is an 8-bit high-speed multiplying digital-to-analogue converter where the output current is a product of the digital number and the input reference current. The full-scale output current is a linear function of the reference current, and is given by the expression:

$$Ifs = 255/256 \times Iref$$

where Iref is the input current at pin 14 (Vref+). The Vref+ and Vref- inputs are taken to the non-inverting and inverting inputs respectively on an internal reference amplifier. Since the Vref-input is taken to OV, the internal feedback maintains a low-impedance, virtual-earth at the Vref+ input pin, and establishes a OV reference at the junction of R68 and CR13. The protection diode CR13 prevents the potential at pin 14 of U12 rising above approximately 0.7V.

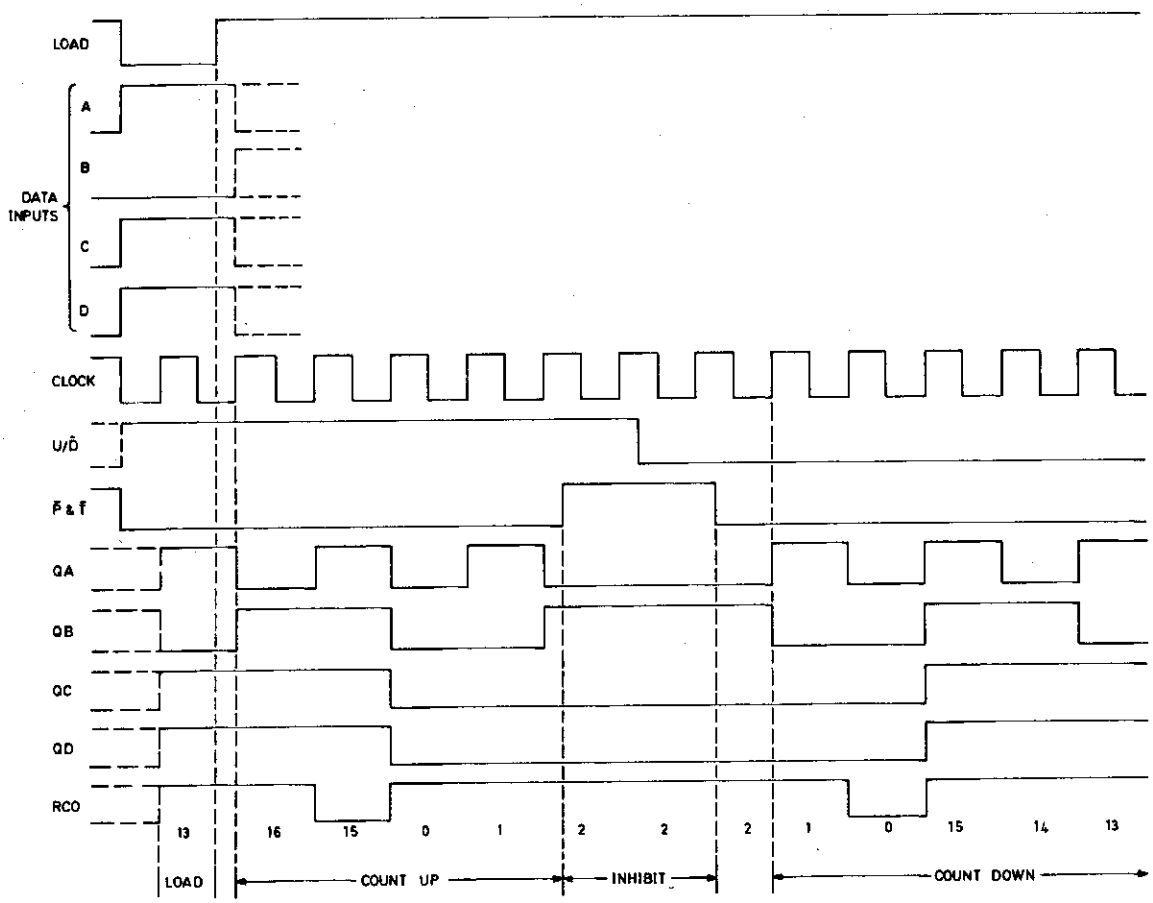



Fig. 7-3 Timing Diagram : Presettable Binary Counter (74LS169)

Phase Comparator

15. The phase comparator uses two high-speed ECL D-type flip-flops U16a, U17a, together with NOR gate U18a. The D inputs of the two flip-flops are taken to OV, the 1 MHz reference signal is used to clock U16a, whilst U17a is clocked by the output signal from the programmed divider. Thus when the positive-going edge of the 1 MHz signal at TP10 clocks U16a, the '0' at the D input results in a '0' at the Q output, and this is applied to one input of U18a.

Similarly, when the positive-going edge of the programmed divider signal at TP9 clocks U17a, the '0' at the D input results in a '0' at the Q output, and this is applied to the remaining input of U18a. When both inputs of U18a are at '0' a '1' is produced at the output, and this is used to reset both U16a and U17b.

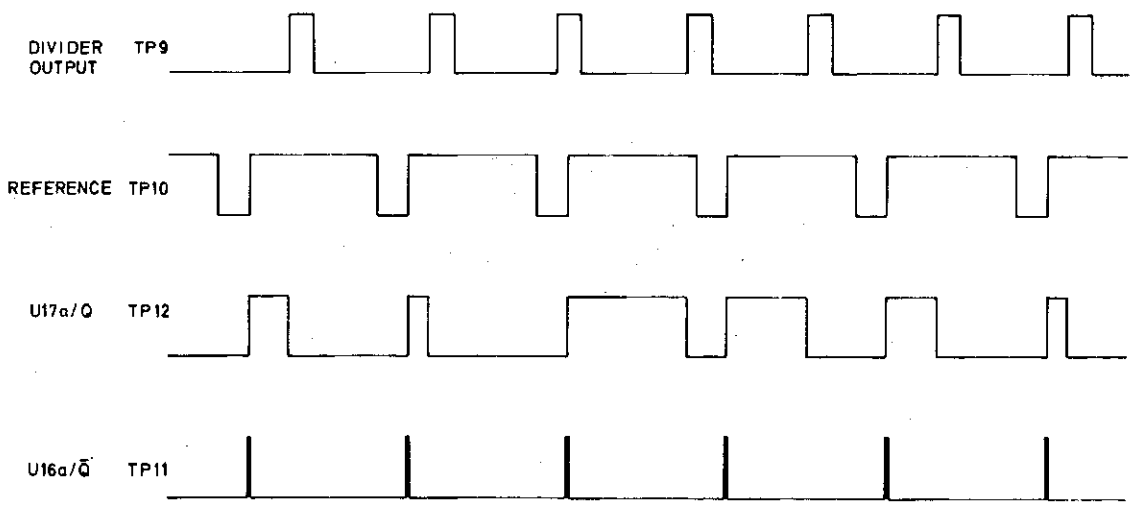



Fig. 7-4 Timing Diagram : Divider Frequency High

16. The timing diagram given in fig. 7-4 shows the situation where the VCO frequency, and hence the divider output frequency is too high. The resulting waveform at the Q output of U17a (TP12) is applied to the fast-lock circuit U20a, which causes a reduction in the VCO varactor voltage (and hence a reduction in the VCO frequency).

17. Under phase-locked conditions, the 4 nanosecond negative-going pulses at the Q output of U17a (fig. 7-6) are too fast to overcome the time constant presented by CR9, R60, C48, and a voltage of approximately +3.8 V is established at the junction of CR9 with CR11.

    Current flow through CR11 is thus prevented, whilst CR12 is forward biased to allow U20a to draw current from the summing node, the level of which is proportional to the output level from the division ratio to voltage converter stage U20b (para. 21).

18. When the VCO frequency is too high, as depicted in fig. 7-4, the relatively wider negative-going pulses at the Q output of U17a, cause a reduction in the voltage level at the junction of CR9 with CR11, and U20a draws current from the summing node via CR11 and R60 to lower the VCO varactor voltage. At the same time, the very narrow positive-going pulses at the $\overline{Q}$ output of U16a cause CR8 to become forward biased, and any current produced by R59 is diverted from the summing node.

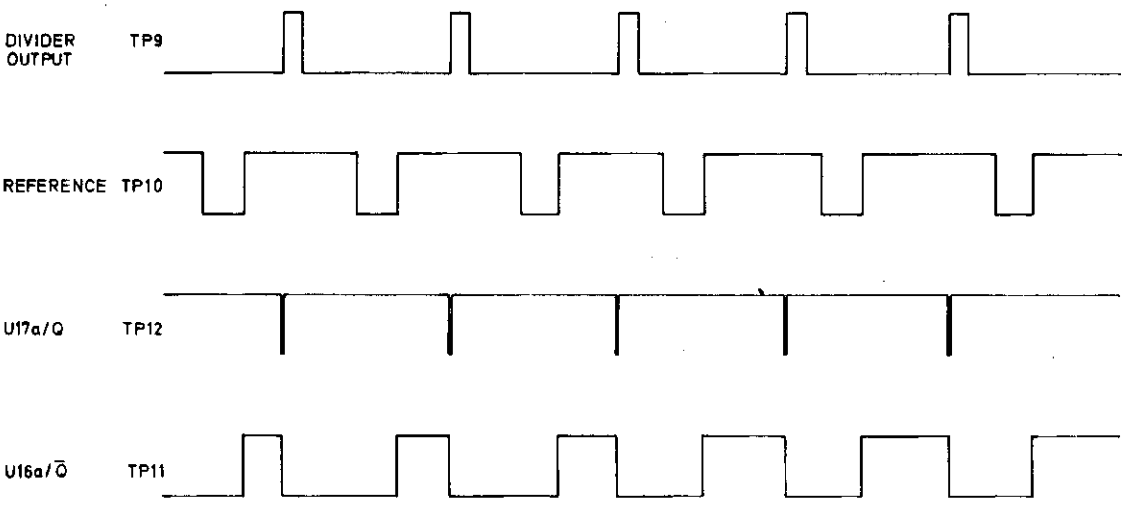



Fig. 7-5 Timing Diagram : Divider Frequency Low

19. The situation where the divider frequency is low is depicted in fig. 7-5. This time the wider positive-going pulses at the $\overline{Q}$ output of U16a allow the current produced by R59 to flow into the summing node to raise the varactor voltage, and hence the VCO frequency. At the same time, the very narrow negative-going pulses at the Q output of U17a prevent current drain from the summing node via CR11 and R60.

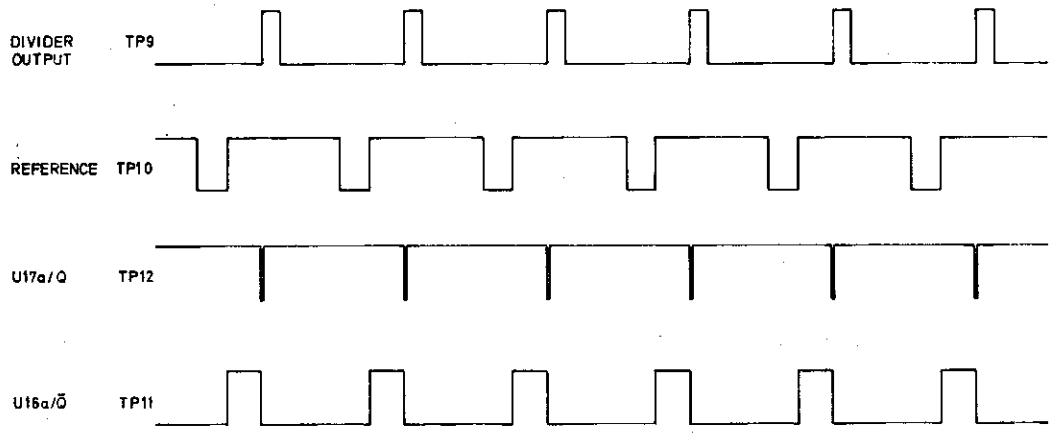



Fig. 7-6 Timing Diagram : Divider & Reference in Phase

20. Fig. 7-6 depicts the in-lock condition, where the two signals are equal in frequency, and where the phasing is such that the duration of the pulses at TP11 is approximately 40 times the duration of the pulses at TP12 (160 nanoseconds and 4 nanoseconds respectively). The effect of this is such that under phase-locked conditions the current fed into the summing node from R59 is equal to that drawn from the node by U20a, no current flows through R65, and a voltage is produced at the output of integrator stage U21 which is inversely proportional to the VCO frequency. This voltage is filtered, level-shifted, inverted and amplified by U19b, and is then applied to the VCO varactor diodes via the loop filters (R83, R87, R88, R89, C63, C64), R92 and L10.

Division Ratio to Voltage Converter

21. This comprises U20b and shottky diodes CR6 and CR7. The feedback loops around operational amplifier U20b (a.c. feedback via C50, d.c. feedback via R62, R50 and CR7) continually strive to maintain the inverting input at the 3.9 V reference level applied to the non-inverting input. Since the positive-going pulses at the $\overline{Q}$ output of U14b are applied to CR6, the higher the division ratio, the shorter the duration of the positive-going pulses, the lower the voltage at the inverting input of U20b and consequently the higher the voltage at the output of U20b.

Fast Lock Detector

22. This circuit, comprising U24a, U24b and U24c, comes into operation following an abrupt change in the drive unit frequency setting. At all other times, the voltages from potential divider R84, R85, R86 ensure that a '1' is present at the outputs of both U24a and U24b (pull-up voltage from R93). This results in a voltage of approximately +20V at the junction of R99, with CR20, and the quad transmission gate U22 is held disabled (U22 is designed to be operated from plus and minus 15 V supplies.

In this application however, the minus supply connection is taken to 0 V, the 0 V connection is taken to +9.1 V, and the positive connection is taken to +20 V. This means that, as far as U22 is concerned, a level of +20V at a control input is regarded as a logic '1', to inhibit switch operation, whilst a level of approximately +9V is regarded as a logic '0', to enable switch operation).

23. When a change of receiver frequency occurs, the voltage at the output of loop amplifier U19b is abruptly taken high for an increase in frequency, or low for a decrease in frequency. This abrupt change is sensed by the limit comparator formed by U24a and U24b such that if the level applied to U24a pin 10/U24b pin 8 exceeds +18 V or falls below +1.6 V, then the output from either U24a or U24b is pulled down to 0 V. This results in a '0' at the output of U24c (TP20) and this is translated to a level of approximately +9 V to enable quad transmission gate U22. The three sections of U22 (a, b and c) close to increase the bandwidth of the loop filter and also to bring the fast lock driver stage U23, Q6, Q7 into operation, to bring about a rapid return to the phase-locked condition.

40.455 MHz to 70.455 MHz VCO

24. The VCO comprises a low-noise, N-chanel FET Q8, tapped inductor L11, and a pair of varactor diodes, CR17 and CR18. The output signal applied to the programmed divider is taken from the drain of Q8, whilst that fed to the mixer board is taken from a low-impedance tap on L11 and is coupled by C71 to the cascode output amplifier stage Q9, Q10.

# FIRST L.O. SYNTHESIZER BOARD A7
(ST 83733)

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R1 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R2 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R3 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R4 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R5 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R6 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R7 | 100 | Variable | | | 923661 |
| R8 | 39 | Metal Oxide | ¼ | 2 | 917062 |
| R9 | 2.2k | Metal Oxide | ¼ | 2 | 916546 |
| R10 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R11 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R12 | 56 | Metal Oxide | ¼ | 2 | 917055 |
| R13 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R14 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R15 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R16 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R17 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R18 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R19 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R20 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R21 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R22 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R23 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R24 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R25 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R26 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R27 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R28 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R29 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R30 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R31 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R32 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R33 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R34 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R35 | 2.2k | Metal Oxide | ¼ | 2 | 916546 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| R36 | 820 | Metal Oxide | ¼ | 2 | 917065 |
| R37 | 820 | Metal Oxide | ¼ | 2 | 917065 |
| R38 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R39 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R40 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R41 | 3.3k | Metal Oxide | ¼ | 2 | 910111 |
| R42 | 150 | Metal Oxide | ¼ | 2 | 910389 |
| R43 | 100 | Variable | | | 923661 |
| R44 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R45 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R46 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R47 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R48 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R49 | 270 | Metal Oxide | ¼ | 2 | 910391 |
| R50 | 2.2k | Metal Oxide | ¼ | 2 | 916546 |
| R51 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R52 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R53 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R54 | 22k | Metal Oxide | ¼ | 2 | 913943 |
| R55 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R56 | 68k | Metal Oxide | ¼ | 2 | 916478 |
| R57 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R58 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R59 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R60 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R61 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R62 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R63 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R64 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R65 | 22 | Metal Oxide | ¼ | 2 | 920743 |
| R66 | 15k | Metal Oxide | ¼ | 2 | 920645 |
| R67 | 390 | Metal Oxide | ¼ | 2 | 916331 |
| R68 | 1.2k | Metal Oxide | ¼ | 2 | 911179 |
| R69 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R70 | 15k | Metal Oxide | ¼ | 2 | 920645 |
| R71 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R72 | 47k | Metal Oxide | ¼ | 2 | 913496 |
| R73 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R74 | 12k | Metal Oxide | ¼ | 2 | 917952 |
| R75 | 10k | Metal Oxide | ¼ | 2 | 914042 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| R76 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R77 | 18k | Metal Oxide | ¼ | 2 | 900994 |
| R78 | 15k | Metal Oxide | ¼ | 2 | 920645 |
| R79 | 15k | Metal Oxide | ¼ | 2 | 920645 |
| R80 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R81 | 47k | Metal Oxide | ¼ | 2 | 913496 |
| R82 | 220 | Metal Oxide | ¼ | 2 | 920751 |
| R83 | 220k | Metal Oxide | ¼ | 2 | 921771 |
| R84 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R85 | 6.8k | Metal Oxide | ¼ | 2 | 910112 |
| R86 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R87 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R88 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R89 | 22 | Metal Oxide | ¼ | 2 | 920743 |
| R90 | 2.2k | Metal Oxide | ¼ | 2 | 916546 |
| R91 | 2.2k | Metal Oxide | ¼ | 2 | 916546 |
| R92 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R93 | 47k | Metal Oxide | ¼ | 2 | 913496 |
| R94 | 220k | Metal Oxide | ¼ | 2 | 921771 |
| R95 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R96 | 68 | Metal Oxide | ¼ | 2 | 916476 |
| R97 | 68 | Metal Oxide | ¼ | 2 | 916476 |
| R98 | 15k | Metal Oxide | ¼ | 2 | 920645 |
| R99 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R100 | 390 | Metal Oxide | ¼ | 2 | 916331 |
| R101 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R102 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R103 | 22 | Metal Oxide | ¼ | 2 | 920743 |
| R104 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R105 | 39 | Metal Oxide | ¼ | 2 | 917062 |
| R106 | 82 | Metal Oxide | ¼ | 2 | 917057 |
| R107 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| Capacitors | | | V | | |
| C1 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C2 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C3 | 1.0 | Tantalum | 35 | 20 | 938405 |
| C4 | 1.0 | Tantalum | 35 | 20 | 938405 |
| C5 | .001 | Ceramic | 500 | 20 | 915243 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| C6 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C7 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C8 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C9 | .001 | Ceramic | 500 | 20 | 915243 |
| C10 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C11 | 0.1 | Polycarbonate | 100 | 10 | 931130 |
| C12 | 10p | Ceramic | 500 | 5 | 921270 |
| C13 | 1.0 | Tantalum | 100 | 20 | 938405 |
| C14 | 1.0 | Ceramic | 500 | 20 | 915243 |
| C15 | 1.0 | Tantalum | 100 | 20 | 938405 |
| C16 | .001 | Ceramic | 500 | 20 | 915243 |
| C17 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C18 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C19 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C20 | 0.1 | Polycarbonate | 100 | 10 | 931130 |
| C21 | 1.0 | Tantalum | 100 | 20 | 938405 |
| C22 | .001 | Ceramic | 500 | 20 | 915243 |
| C23 | 0.1 | Polycarbonate | 100 | 10 | 931130 |
| C24 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C25 | .001 | Ceramic | 500 | 20 | 915243 |
| C26 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C27 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C28 | 6.8 | Tantalum | 40 | 10 | 931178 |
| C29 | .001 | Ceramic | 500 | 20 | 915243 |
| C30 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C31 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C32 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C33 | 6.8 | Tantalum | 40 | 10 | 931178 |
| C34 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C35 | .001 | Ceramic | 500 | 20 | 915243 |
| C36 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C37 | 0.1 | Polycarbonate | 100 | 10 | 931130 |
| C38 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C39 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C40 | 6.8 | Tantalum | 40 | 10 | 931178 |
| C41 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C42 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C43 | 6.8 | Tantalum | 40 | 10 | 931178 |
| C44 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C45 | 6.8 | Tantalum | 40 | 10 | 931178 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| C46 | .001 | Ceramic | 500 | 20 | 915243 |
| C47 | 0.1 | Polycarbonate | 100 | 10 | 931130 |
| C48 | 100p | Ceramic | 500 | 10 | 917417 |
| C49 | 1.0 | Tantalum | 100 | 20 | 938405 |
| C50 | 1.0 | Tantalum | 100 | 20 | 938405 |
| C51 | 100p | Ceramic | 500 | 10 | 917417 |
| C52 | 22p | Ceramic | 500 | 5 | 913986 |
| C53 | .01 | Ceramic | 250 | -20+40 | 940315 |
| C54 | 100p | Ceramic | 500 | 10 | 917417 |
| C55 | .01 | Ceramic | 250 | -20+40 | 940315 |
| C56 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C57 | .047 | Polycarbonate | 250 | | 935141 |
| C58 | .0015 | Ceramic | 100 | 10 | 939929 |
| C59 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C60 | .01 | Ceramic | 250 | -20+40 | 940315 |
| C61 | .001 | Ceramic | 500 | 20 | 915243 |
| C62 | .001 | Ceramic | 500 | 20 | 915243 |
| C63 | 1.0 | Polycarbonate | 100 | 10 | 931133 |
| C64 | .033 | Polycarbonate | 250 | 10 | 939695 |
| C65 | 0.1µF | Polycarbonate | 100 | 10 | 931130 |
| C66 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C67 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C68 | .001 | Ceramic | 500 | 20 | 915243 |
| C69 | .001 | Ceramic | 500 | 20 | 915243 |
| C70 | 6.8 | Tantalum | 40 | 10 | 931178 |
| C71 | .001 | Ceramic | 500 | 20 | 915243 |
| C72 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C73 | .01 | Ceramic | 250 | -20+40 | 900067 |
| C74 | .001 | Ceramic | 500 | 20 | 915243 |
| C75 | 10p | Ceramic | 500 | 5 | 921270 |
| C76 | | Not Used | | | |
| C77 | 0.1 | Polycarbonate | 100 | 10 | 931130 |
| C78 | 4.7 | Tantalum | 35 | 20 | 914026 |
| C79 | .001 | Ceramic | 100 | 20 | 940037 |
| C80* | .001 | Ceramic | 500 | 20 | 915243 |

Diodes

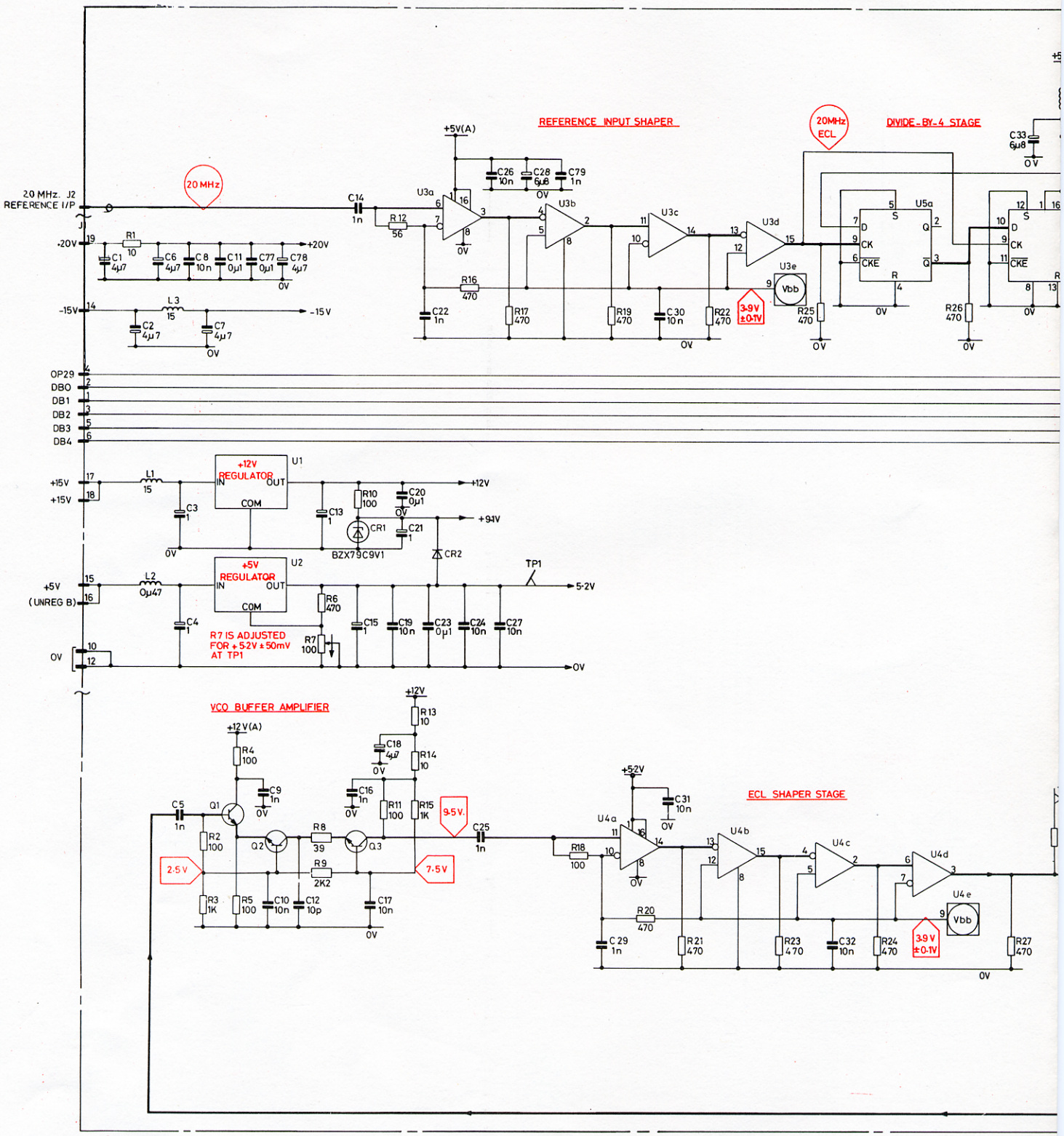
| | | |
|---|---|---|
| CR1 | BZX79C9V1 | 921751 |
| CR2 | 1N4001 | 923563 |
| CR3 | HP5082-2811 | 919460 |
| CR4 | IN4149 | 914898 |
| CR5 | 1N4149 | 914898 |

*C80 is not used if U6 11C91 is fitted. Ref Figs 7.7 and 7.9.

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| CR6 | | HP5082-2811 | | | 919460 |
| CR7 | | HP5082-2811 | | | 919460 |
| CR8 | | HP5082-2811 | | | 919460 |
| CR9 | | IN4149 | | | 914898 |
| CR10 | | HP5082-2811 | | | 919460 |
| CR11 | | 1N4149 | | | 914898 |
| CR12 | | 1N4149 | | | 914898 |
| CR13 | | IN4149 | | | 914898 |
| CR14 | | IN4149 | | | 914898 |
| CR15 | | IN4149 | | | 914898 |
| CR16 | | IN4149 | | | 914898 |
| CR17 | | KV2201 | | | 938614 |
| CR18 | | KV2201 | | | 938614 |
| CR19 | | IN4149 | | | 914898 |
| CR20 | | IN4149 | | | 914898 |
| **Transistors** | | | | | |
| Q1 | | NPN 2N 2369 | | | 906842 |
| Q2 | | NPN 2N 2369 | | | 906842 |
| Q3 | | NPN 2N 2369 | | | 906842 |
| Q4 | | NPN 2N 2369 | | | 906842 |
| Q5 | | NPN BC109 | | | 923234 |
| Q6 | | NPN BC 109 | | | 923234 |
| Q7 | | PNP ZTX 550L | | | 937503 |
| Q8 | | 2N3823 | | | 938592 |
| Q9 | | NPN 2N 3866 | | | 917219 |
| Q10 | | NPN 2N 3866 | | | 917219 |
| **Integrated Circuits** | | | | | |
| U1 | | 7812 | | | 933987 |
| U2 | | 340 | | | 939921 |
| U3 | | 10115 | | | 935262 |
| U4 | | 10115 | | | 935262 |
| U5 | | 10231 | | | 935264 |
| U6* | | 12012 or 11C91 | | | 941051 or 939928 |
| U7 | | 74LS27 | | | 931631 |
| U8 | | 74LS169 | | | 939895 |
| U9 | | RMSL019/A | | | AD80763 |
| U10 | | 4527 | | | 931016 |

* Ref Figs. 7.7 and 7.9 for alternative circuits

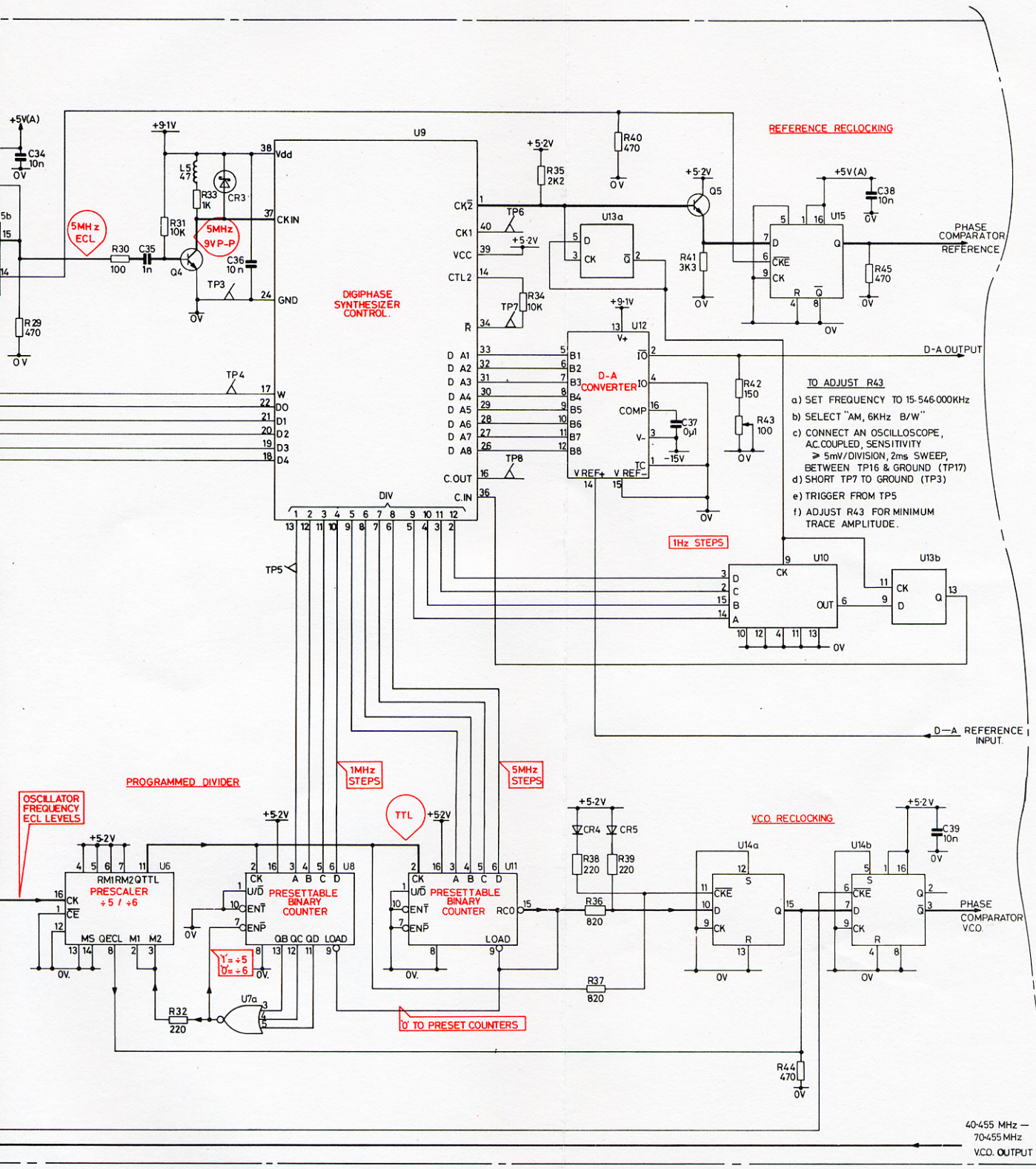
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| U11 | | 74LS169 | | | 939895 |
| U12 | | 08 | | | 939896 |
| U13 | | 4013 | | | 935562 |
| U14 | | 10231 | | | 935264 |
| U15 | | 10231 | | | 935264 |
| U16 | | 10231 | | | 935264 |
| U17 | | 10231 | | | 935264 |
| U18 | | 10102 | | | 935265 |
| U19 | | 324 | | | 933619 |
| U20 | | 324 | | | 933619 |
| U21 | | 518 | | | 935269 |
| U22 | | 201 | | | 934880 |
| U23 | | 3140 | | | 932204 |
| U24 | | 339 | | | 925952 |
| **Transformers** | | | | | |
| T1 | | RF Wideband | | | AT81411 |
| **Inductors** | | | | | |
| L1 | 15µH | Choke | | | 938955 |
| L2 | .47µH | Choke | | | 939693 |
| L3 | 15µH | Choke | | | 938955 |
| L4 | 1µH | Choke | | | 938966 |
| L5 | 47µH | Choke | | | 939160 |
| L6 | 1µH | Choke | | | 938966 |
| L7 | .47µH | Choke | | | 939693 |
| L8 | 1µH | Choke | | | 938966 |
| L9 | 1.5µH | Choke | | | 938967 |
| L10 | 6.8µH | Choke | | | 939694 |
| L11 | | Coil Assembly | | | AT81189 |
| **Connectors** | | | | | |
| J1 | | Plug 20-way | | | 938675 |
| J2 | | Plug co-axial 50 ohms | | | 938429 |
| J3 | | Plug co-axial 50 ohms | | | 938429 |
| J4 | | Plug co-axial 50 ohms | | | 938429 |



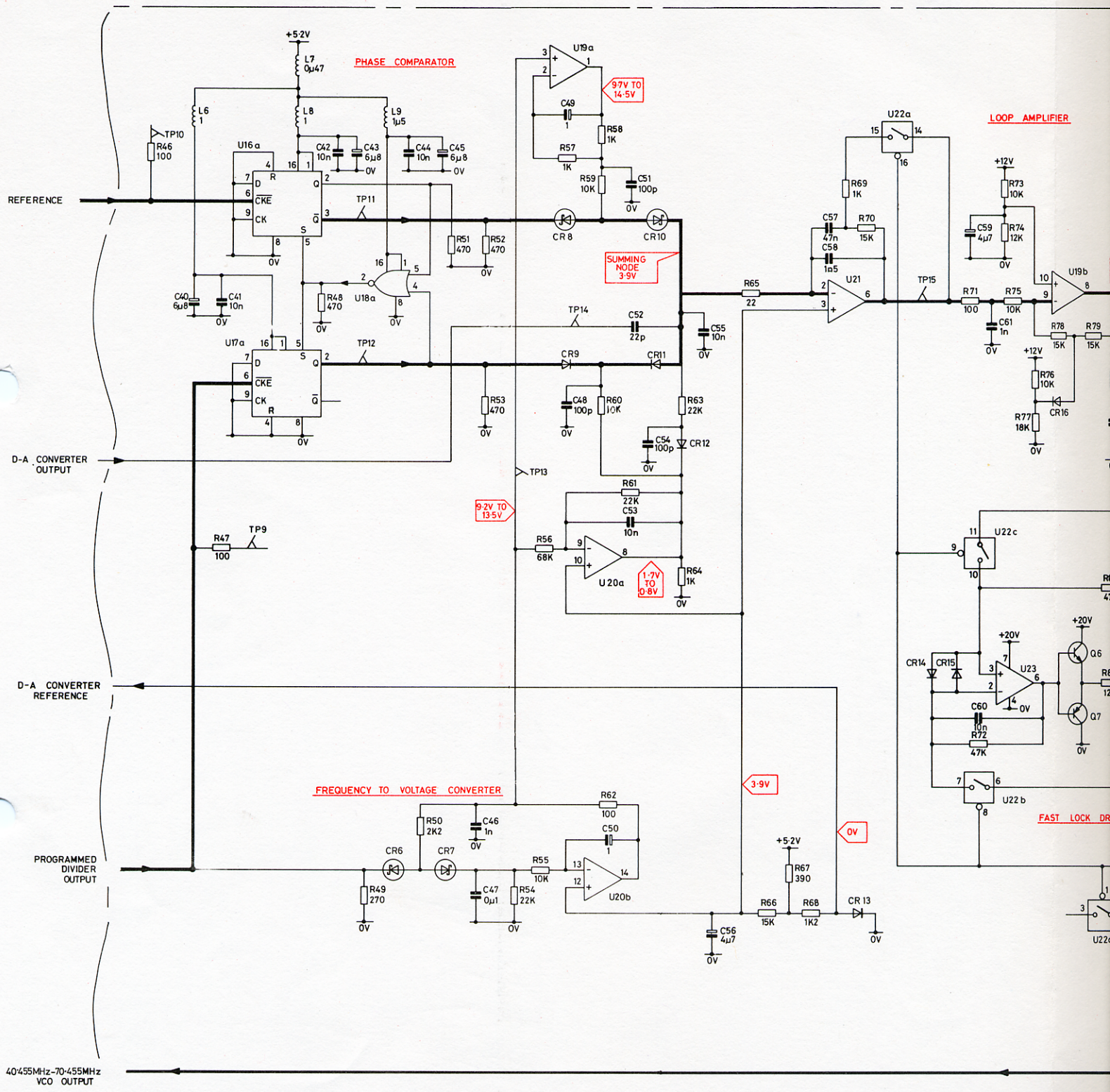

RACAL

| TH 3416 | DC 83733/1/1 |
|---|---|
| 1 | 3 |

| TH 3416 | DC 83733/1/2 |
|---|---|
| 1 | 3 |



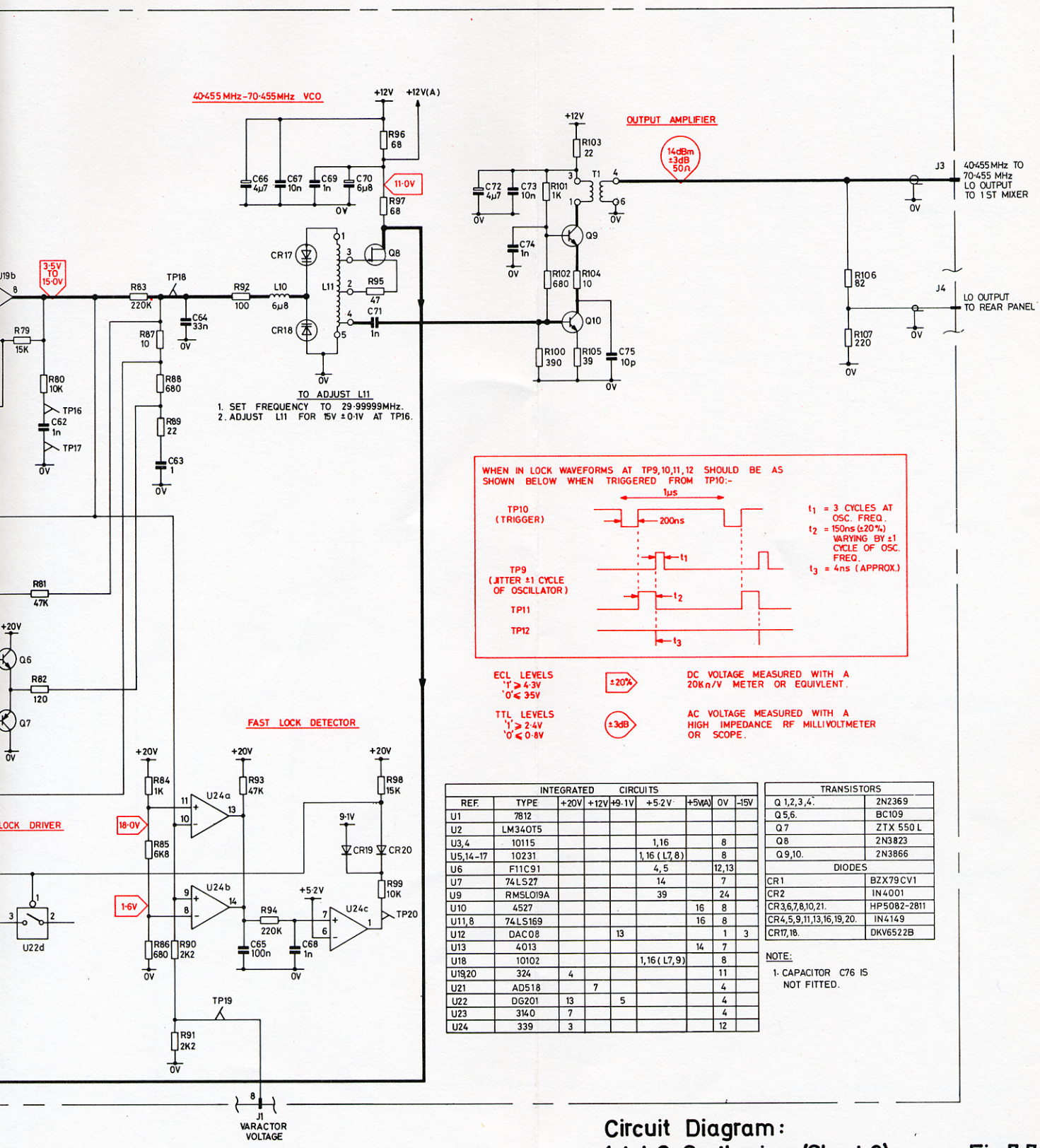

**Circuit Diagram :**
**1st L.O. Synthesizer (Sheet 1)** Fig. 7·7




RACAL

| TH3416 | DC 83733/2/1 |
|---|---|
| 1 3 | |


| TH3416 | DC83733/2/2 |
|---|---|
| 1 3 | |

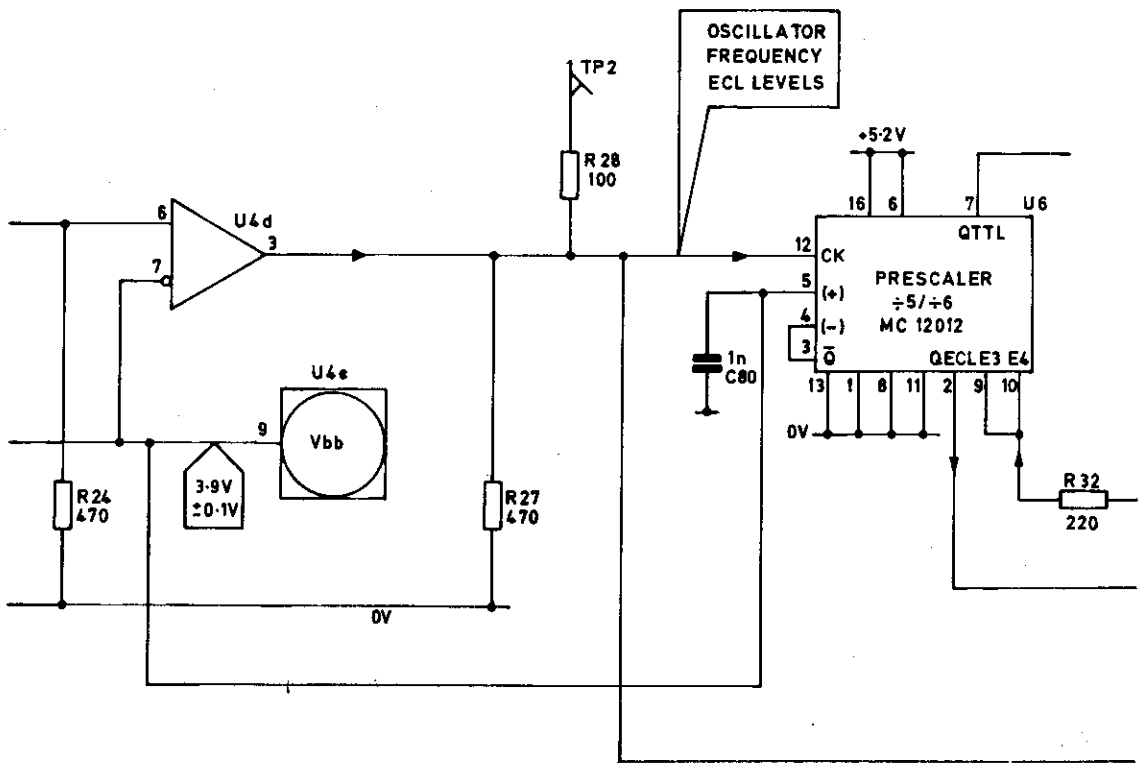



| INTEGRATED CIRCUITS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| REF. | TYPE | +20V | +12V | +9·1V | +5·2V | +5VA | 0V | -15V |
| U1 | 7812 | | | | | | | |
| U2 | LM340T5 | | | | | | | |
| U3,4 | 10115 | | | | 1,16 | | 8 | |
| U5,14–17 | 10231 | | | | 1,16 (L7,8) | | 8 | |
| U6 | F11C91 | | | | 4,5 | | 12,13 | |
| U7 | 74LS27 | | | | 14 | | 7 | |
| U9 | RMSLO19A | | | | 39 | | 24 | |
| U10 | 4527 | | | | | 16 | 8 | |
| U11,8 | 74LS169 | | | | | 16 | 8 | |
| U12 | DAC08 | | | 13 | | | 1 | 3 |
| U13 | 4013 | | | | | 14 | 7 | |
| U18 | 10102 | | | | 1,16 (L7,9) | | 8 | |
| U19,20 | 324 | 4 | | | | | 11 | |
| U21 | AD518 | | 7 | | | | 4 | |
| U22 | DG201 | 13 | | 5 | | | 4 | |
| U23 | 3140 | 7 | | | | | 4 | |
| U24 | 339 | 3 | | | | | 12 | |

| TRANSISTORS | |
|---|---|
| Q 1,2,3,4. | 2N2369 |
| Q 5,6. | BC109 |
| Q 7 | ZTX 550 L |
| Q 8 | 2N3823 |
| Q 9,10. | 2N3866 |
| DIODES | |
| CR 1 | BZX79 CV1 |
| CR 2 | IN4001 |
| CR 3,6,7,8,10,21. | HP5082-2811 |
| CR 4,5,9,11,13,16,19,20. | IN4149 |
| CR 17,18. | DKV6522B |

NOTE:
1. CAPACITOR C76 IS NOT FITTED.

**Circuit Diagram:**
**1st L.O. Synthesizer (Sheet 2)** Fig. 7·7

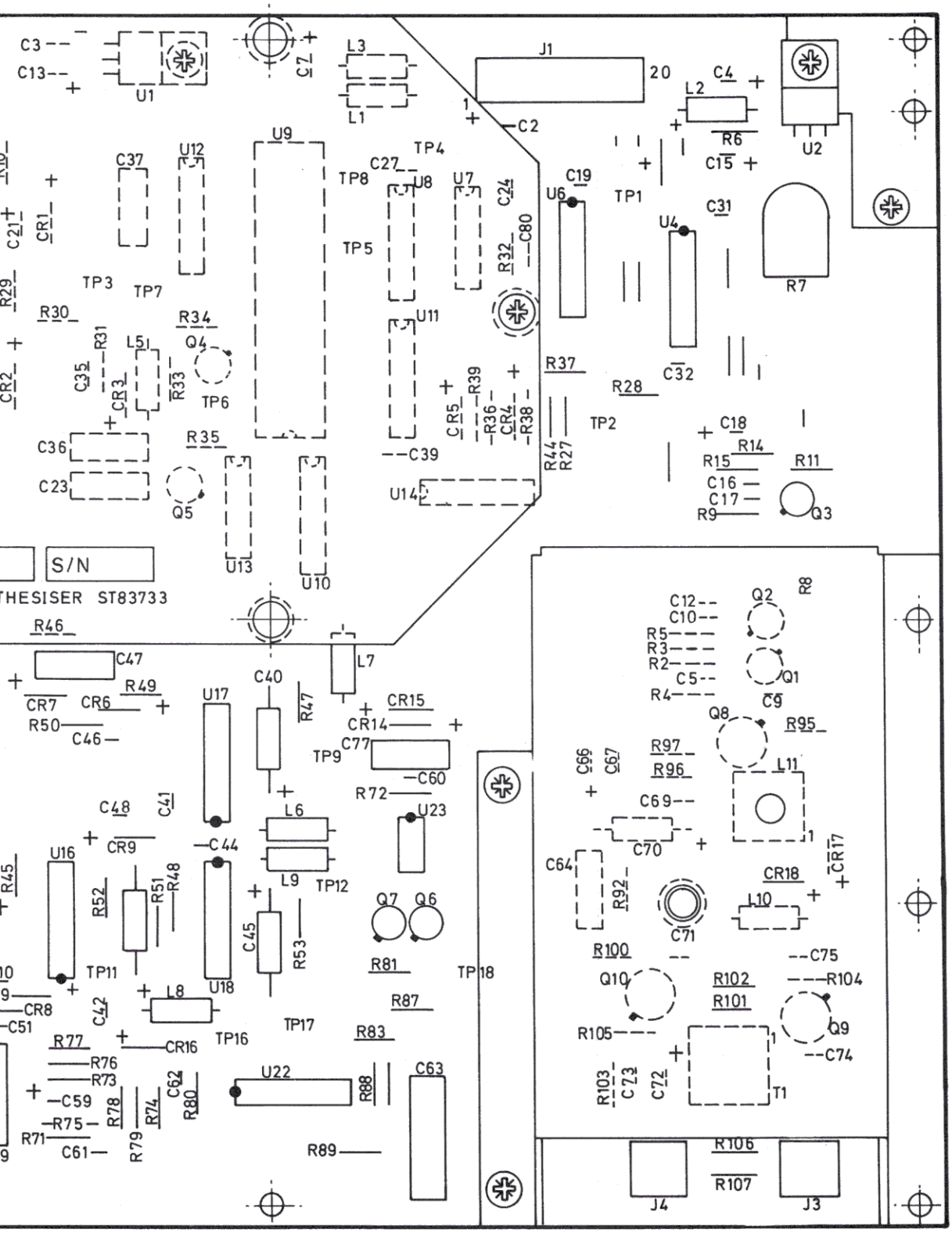



ALL OTHER CONNECTIONS ARE AS
SHOWN ON FIG. 7-7

CIRCUIT : ALTERNATIVE PRESCALER MC 12012 FIG 7-8

RA1792

C28
C26
C34
U3
J2
C14
C79
R22
R12
R16
C22
R17
R19
R25
U5
C30
U15
TP19
C33
R40
R41
TP20
L4
C38
U24
R94
C65
R98
CR19
CR20
R99
R90
R91
C68
R93
R86
R85
R84
TP10
C78
R54
R55
U20
CR13
R43
C50
R61
R64
C53
R42
CR12
R60
CR11
TP14
C52
C54
C55
R63
R67
R68
R65
C57
C58
R66
C56
U21
R58
R57
C49
TP15
R70
R69
C11
C20




**Component Layout :**
**1st L.O. Synthesizer Board A7(LSI) Fig.7-9**

# CHAPTER 8

# SECOND L.O./BFO SYNTHESIZER A8

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| | CIRCUIT DESCRIPTION | |
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## ILLUSTRATIONS


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| 8-5 | Component Layout : Second L.O./BFO Synthesizer | |

# CHAPTER 8

# SECOND L.O/B.F.O. SYNTHESIZER A8

## INTRODUCTION

1. The Second L.O. Synthesizer operates, as standard, from an input frequency of 5 MHz, supplied by the A11 Frequency-Standard module. Alternatively, a 5 MHz TXCO module may be fitted to this board. If neither of these options are used, than an external reference frequency must be applied to J1. This is link-selectable for external frequencies of 1 MHz, 5 MHz or 10 MHz. If either the A11 module or the on-board TXCO are used, then a frequency reference is available using J1 as an output.

2. The synthesizer gives the following main outputs:

   20 MHz for First L.O. synthesizer board
   40 MHz for Second mixer board
   455 kHz ± 8 kHz BFO (Offset programmable in 10 Hz steps)
   Out-of-lock reference voltage for BITE use.

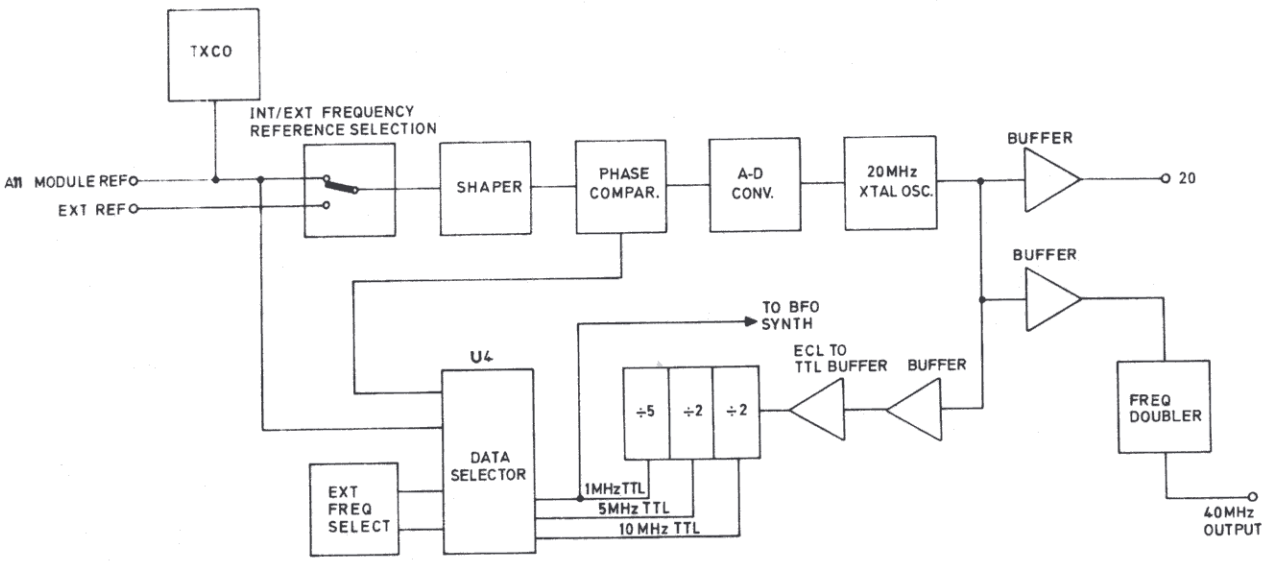
## FUNCTIONAL DESCRIPTION

3. The A8 Synthesizer module may be conveniently regarded as two distinct sections: The Second L.O.Synthesizer, and the BFO Synthesizer. The functional description (and the circuit description following) will use this approach, bearing in mind that the two sections are on the same circuit board.

### Second L.O. Synthesizer

4. Fig. 8-1 shows this part of the A8 module in block-diagram form. After frequency-reference selection (see para. 1) the reference chosen is shaped (Q4 - Q6), and applied to one input of the phase comparator, U3. The second comparator input is taken from the buffered and divided crystal oscillator output. The phase comparator output is in the form of pulses of differing width, depending upon the prevailing relationship between the input frequency reference and the on-board oscillator frequency.

5. The phase comparator output is converted by Q7 - Q9 into an analogue voltage which is used to alter the frequency of the 20 MHz oscillator (U22d). This is once again fed back as reference to the phase comparator for further comparison until the D-A converter 'tunes' the 20 MHz oscillator into lock with the reference frequency. In cases where externally applied reference frequencies are used and these differ from the normal 5 MHz (either 1 MHz or 10 MHz), U6 and U7 provide the appropriate internal frequencies via U4 to allow correct conditions at the phase comparator. A 1 MHz frequency reference is taken to the BFO section from U6.




RACAL
TH 3416

Block Diagram:
2nd LO Sythesizer

Fig. 8.1

Fig. 8-1

BFO Synthesizer

6. Fig. 8-2 shows the BFO synthesizer section of the A8 module in block-diagram form. 1 MHz frequency reference is taken from the 2nd L.O. synthesizer section, and divided successively by 100 and 20, to provide a final reference of 500 Hz. This is applied to one input of the phase comparator, U10, the other input being supplied by a programmable divider comprising U12-U19. The output from the phase comparator is digital, representing the difference between the external reference and the internally divided signal.

7. Q15-Q17 form a digital to analogue converter, the resulting voltage being used to control the frequency of the 22.75 MHz oscillator (Q18). The oscillator output is buffered and shaped before being applied to the programmable divider chain. This chain allows BFO offset to be programmed in 10 Hz steps to a maximum of $\pm$ 8 kHz. The output of this chain is referred to the Phase Comparator (U10), the difference once again controlling Q18. Thus for each change in the divider chain, an oscillator frequency change must occur to maintain the divider output (and thus the comparator input) at 500 Hz.

8. In addition to being applied to the programmable divider chain, after buffering and shaping, Q18 output is divided by 50 and leaves the board at J4 at 455 kHz $\pm$8 kHz, this being the BFO output.

CIRCUIT DESCRIPTION

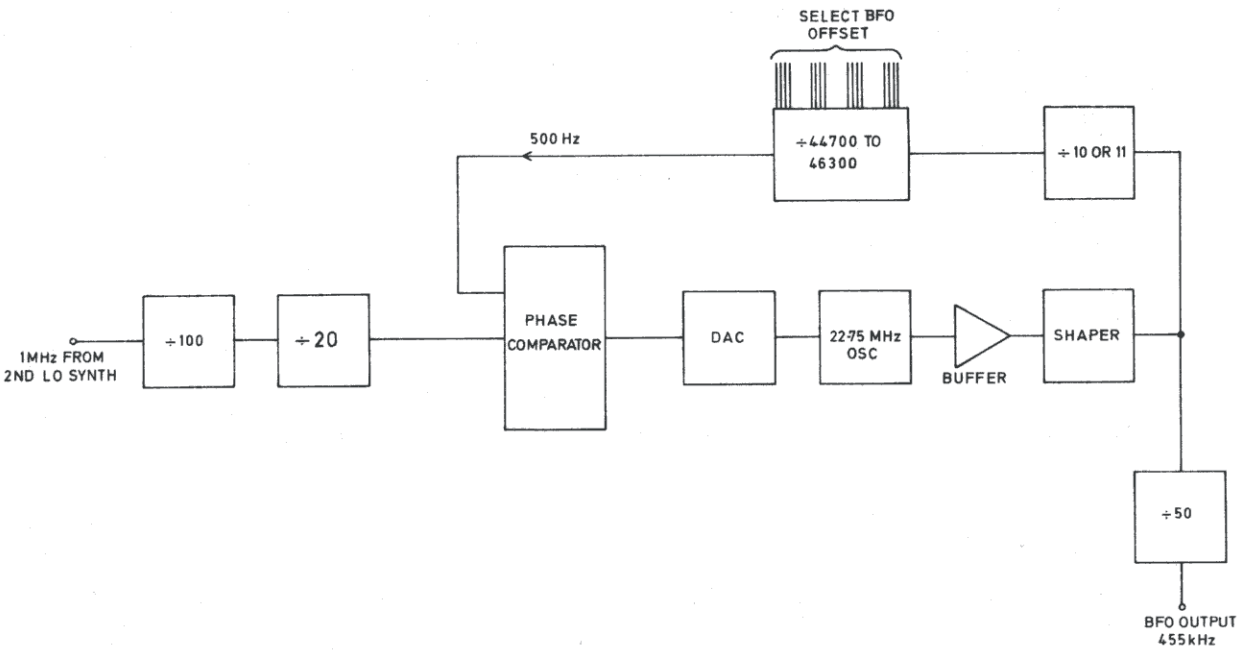
SECOND L.O. SYNTHESIZER

9. Fig. 8-4 (at the end of this chapter) shows the circuit for the second local oscillator synthesizer section of the A8 module.

Frequency Reference

10. Normally the RA1792 uses a 5 MHz reference from the A11 frequency standard module (Chapter 12). It is, however, possible to use an on-board 5 MHz crystal oscillator in a crystal oven (TXCO), which receives its power supply from regulator U1. This incorporates a remote shutdown facility. Alternatively, an external reference may be used and this may be 1 MHz, 5 MHz or 10 MHz, being selected on the synthesizer board by links 1 & 2 (see Para. 19).

11. To select internal reference, either A11 or TXCO, a voltage smaller than 0.4 V is applied to A8J6 pin 3. This allows U1 to operate (Q1 off), supplying the TXCO (if used) and Q21 for reference from the A11 module (standard). When external reference is used, a voltage larger than +2.5 V is applied to A7J6 pin 3, where upon Q1 is switched on, shutting down U1. This voltage is also applied to U2 pins 1 & 2, causing U2 output to go low and switch off the internal reference via CR3 acting on Q5. The external reference signal is passed by Q4, as CR2 is reverse biased, U2d applying the inverse of U2a output. Q4 and Q5 sharing a common collector circuit, act as an OR gate, allowing one or other of the chosen signals to pass. When an internal reference is used, applying a voltage of greater than +2.5 V to A8J6 pin 3 causes remote shutdown.




RACAL
TH 3416

Block Diagram:
BFO Synthesizer

Fig.8.2

Fig. 8-2

12. An external frequency reference, when used, is applied to J1. When an internal reference is used, however, J1 provides an output of 1 MHz, buffered by Q2 and Q3, switched through U5 from U6.

13. Q6 provides shaping for the incoming reference signal, squaring it to make it suitable for use by U3, the phase comparator.

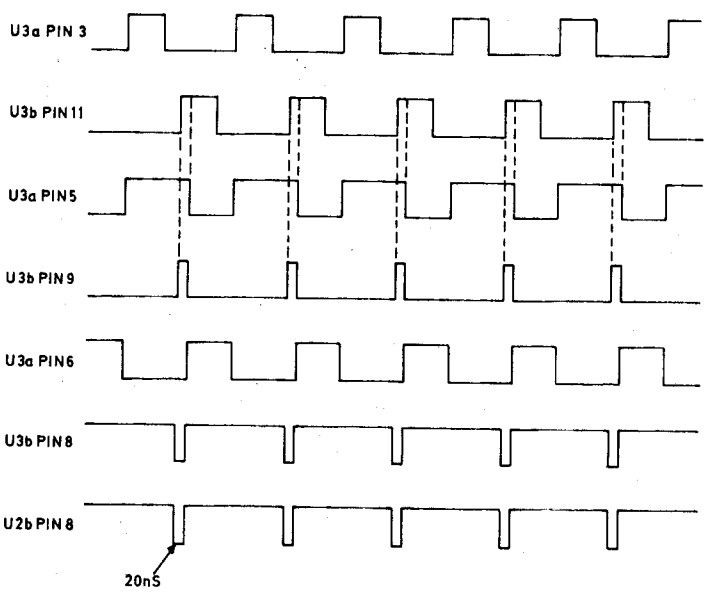



Fig. 8-3 Phase Comparator Waveforms

Phase Comparator

14. Referring to fig. 8-3, the chosen reference frequency, either 1 MHz, 5 MHz or 10 MHz, having been squared, is used as a clock signal into U3a pin 3. U3 is a dual D-type positive edge triggered flip-flop. As the incoming waveform rises, the level at pin 2, the D input (tied to +5 V), is transformed to the Q output, U3a pin 5, as shown.

15. The on-board 20 MHz local oscillator output, after division to match the incoming reference frequency is applied to U3b pin 11, the U3b clock input. When the system is out of lock, one of these two clock signals must arrive first and raise its Q output. In this example, fig. 8-3 shows that it was the U3a clock, with pin 5 going high immediately. At some later time the U3b clock pulse arrives at pin 11, pin 9 now going high. However, the two Q outputs, pins 5 and 9 are NAND gated by U2b, the result clearing both flip-flops. As the delay time of R32 and C20, plus the delay through U2b, is approximately 20nS, both signals will overlap for this length of time, giving the 20nS-wide pulse at U2b pin 8. In effect, either clock may arrive first, its Q output being raised immediately, and this condition will prevail until 20nS after the arrival of the other clock.

D-A converter

16. The D-A Converter consists of Q7, Q8 and Q9 plus associated components. U3a pin 6, a $\overline{Q}$ output, is connected to Q7 emitter and U3b pin 8, the other $\overline{Q}$ output is connected to Q9 emitter. Referring again to fig. 8-3, when U3a pin 6 is low, Q7 is switched on, and in turn switches on Q8 which sources current into the oscillator control line, raising the voltage and increasing the local-oscillator frequency. Whilst U3b pin 8 is low, Q9 is switched on and cancels the effect of Q8. In a condition where the clock at U3b pin 11 arrives first (indicating that the local oscillator frequency is too high), then Q9 would conduct, sinking current from the oscillator control line, thus reducing the oscillator frequency. When the reference and the local oscillator are in lock, both clock signals arrive simultaneously, and both of the U3-$\overline{Q}$ outputs are low for 20nS. The effect of this is to switch on both Q8 and Q9 when the signal is low, thus cancelling their effect and to switch off Q8 and Q9 when the signal is high, once again cancelling their effect.

Loop Filter

17. C25, C26 and C32 with R39 form the loop filter, filtering the sudden voltage changes of Q8 and Q9 into a sufficiently smooth voltage level. This is established in the range 6-11 V and is monitored by BITE via U23, a voltage buffer.

20 MHz Crystal Oscillator

18. The 20 MHz local oscillator provides 20 MHz to the divider chain which is then fed back to provide phase locking with an incoming reference signal. The oscillator provides a buffered 20 MHz output via J8 to the First L.O. Synthesizer (module A7). A 40 MHz output is provided by Q11 circuit, a frequency doubler, for use by the second mixer (module A3).

Divider Chain

19. After buffering, the 20 MHz signal is changed from ECL levels to TTL levels by Q10 and then passes into the divider chain formed by U7a, U7b and U6, to give division of the input 20 MHz by 2 (10 MHz) by 4 (5 MHz) and by 20 (1 MHz). These three signals are applied to U4 inputs. U4 switches the divider frequencies, providing a reference for the phase-locked loop, of 1 MHz, 5 MHz or 10 MHz, according to the code on pins 9, 10 and 11. Pin 9 is high when external is selected (A8J6 pin 3), and the reference frequency is set on pins 10 and 11 by links 1 and 2, 1 MHz being selected by connection of link 2 only, and 10 MHz selected by connection of link 1 only. The selected frequency, chosen to equal the input reference frequency, is then applied to U3b pin 11. For operation from this point, see para. 14.

1 MHz is permanently available from U6 pin 12 in the divider chain, for use by the BFO synthesizer section of this board, to be described next.

BFO SYNTHESIZER

20. Fig. 8.4 (at the end of this Chapter) shows the circuit for the BFO synthesizer section of the A8 module.

Phase Comparator

21. The 1 MHz reference frequency input is divided by 100 and then 20, to provide a reference frequency of 500 Hz. This is applied to U10, the phase comparator. The 500 Hz output from the programmable divider U12 - U19 is applied to U10 pin 11. Operation of the phase comparator is similar to that described in paras. 14 and 15 (this chapter), except that the device and pin numbers differ, as do the frequencies involved.

D-A Converter

22. Operation of this circuit is similar to that described in para. 16 (this chapter), except that the transistor numbers differ. BFO out-of-lock information is available at A8J5 pin 2 from U11d, and loop voltage variation is available, buffered by U24, at A8J5 pin 1. The in-lock voltage at this point is 8 V ± 0.5 V when there is no BFO offset (BFO running at 455 kHz).

Loop Filter and 22.75 MHz Oscillator

23. C50, C51, R65 and L3 form the loop filter which provides a DC voltage for operation of CR6 and CR7, and thus controls the 22.75 MHz oscillator. The oscillator uses FET Q18 and associated components. This oscillator changes frequency under control of the loop filter voltage so that whatever BFO offset is chosen, the programmable divider chain will always

output 500 Hz. The oscillator range is from 22.35 MHz to 23.15 MHz. Provision has been made for remote switching of the BFO oscillator via U21, an optically coupled device. A low on this line enables the BFO oscillator. The oscillator output is buffered by FET Q19 and applied to the programmable divider chain via C72.

Programmable Dividers

24. The divider chain allows for a total range of 16 kHz at the BFO output, effectively providing ±8 kHz around the 455 kHz centre frequency. The divider accepts minimum steps of 10 Hz and is programmed in decades. The total division range is from 44700 to 46300, which allows the input frequency to range from 22.35 MHz to 23.15 MHz, to maintain a divided output of 500 Hz. The 500 Hz output is applied to U10b, pin 11 for comparison with the input reference and subsequent phase locking of the system.

BFO Output

25. The signal from Q18, the local oscillator, is buffered by Q19 and shaped by Q20 before application to a TTL ÷ 50 circuit, U20. The Qd output of U20 is applied to a low-pass filter built around L6, and is available at A8J4.

## SECOND LO/BFO SYNTHESIZER BOARD A8 (ST 82916)

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R1 | 20k | Variable | | | 938593 |
| R2 | 33 | Metal Oxide | ¼ | 2 | 917060 |
| R3 | 1k8 | Metal Oxide | ¼ | 2 | 911148 |
| R4 | 6k8 | Metal Oxide | ¼ | 2 | 910112 |
| R5 | 2k2 | Metal Oxide | ¼ | 2 | 916546 |
| R6 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R7 | 4k7 | Metal Oxide | ¼ | 2 | 913490 |
| R8 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R9 | 33 | Metal Oxide | ¼ | 2 | 917060 |
| R10 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R11 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R12 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R13 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R14 | | Not Used | | | |
| R15 | | Not Used | | | |
| R16 | | Not Used | | | |
| R17 | | Not Used | | | |
| R18 | 3k3 | Metal Oxide | ¼ | 2 | 910111 |
| R19 | 1k8 | Metal Oxide | ¼ | 2 | 911148 |
| R20 | 3k3 | Metal Oxide | ¼ | 2 | 910111 |
| R21 | 1k8 | Metal Oxide | ¼ | 2 | 911148 |
| R22 | 820 | Metal Oxide | ¼ | 2 | 917065 |
| R23 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R24 | 4k7 | Metal Oxide | ¼ | 2 | 913490 |
| R25 | 4k7 | Metal Oxide | ¼ | 2 | 913490 |
| R26 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R27 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R28 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R29 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R30 | | Not Used | | | |
| R31 | | Not Used | | | |
| R32 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R33 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R34 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R35 | 820 | Metal Oxide | ¼ | 2 | 917065 |
| R36 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R37 | 3k3 | Metal Oxide | ¼ | 2 | 910111 |
| R38 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R39 | 2k2 | Metal Oxide | ¼ | 2 | 916546 |
| R40 | 470 | Metal Oxide | ¼ | 2 | 920758 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R41 | 3k3 | Metal Oxide | ¼ | 2 | 910111 |
| R42 | | Not Used | | | |
| R43 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R44 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R45 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R46 | 56 | Metal Oxide | ¼ | 2 | 917055 |
| R47 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R48 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R49 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R50 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R51 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R52 | 220 | Metal Oxide | ¼ | 2 | 910390 |
| R53 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R54 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R55 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R56 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R57 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R58 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R59 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R60 | 2k2 | Metal Oxide | ¼ | 2 | 916546 |
| R61 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R62 | 3k3 | Metal Oxide | ¼ | 2 | 910111 |
| R63 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R64 | 2k2 | Metal Oxide | ¼ | 2 | 916546 |
| R65 | 18k | Metal Oxide | ¼ | 2 | 900994 |
| R66 | 560 | Metal Oxide | ¼ | 2 | 920831 |
| R67 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R68 | 560 | Metal Oxide | ¼ | 2 | 920831 |
| R69 | 330 | Metal Oxide | ¼ | 2 | 915690 |
| R70 | 150 | Metal Oxide | ¼ | 2 | 910389 |
| R71 | | Not Used | | | |
| R72 | 4k7 | Metal Oxide | ¼ | 2 | 913490 |
| R73 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R74 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R75 | 1k8 | Metal Oxide | ¼ | 2 | 911148 |
| R76 | 820 | Metal Oxide | ¼ | 2 | 917065 |
| R77 | 820 | Metal Oxide | ¼ | 2 | 917065 |
| R78 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R79 | 3k3 | Metal Oxide | ¼ | 2 | 910111 |
| R80 | 2k2 | Metal Oxide | ¼ | 2 | 916546 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R81 | 4k7 | Metal Oxide | ¼ | 2 | 913490 |
| R82 | 3k3 | Metal Oxide | ¼ | 2 | 910111 |
| R83 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R84 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| Capacitors | | | V | | |
| C1 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C2 | 100p | Mica | 500 | 5 | 943143 |
| C3 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C4 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C5 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C6 | 0.047 | Ceramic | 50 | 20 | 938511 |
| C7 | 0.047 | Ceramic | 50 | 20 | 938511 |
| C8 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C9 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C10 | 0.001 | Ceramic | 50 | 20 | 938408 |
| C11 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C12 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C13 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C14 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C15 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C16 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C17 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C18 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C19 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C20 | 12p | Mica | 350 | ±1p | 902139 |
| C21 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C22 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C23 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C24 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C25 | 3.3 | Tantalum | 16 | 10 | 930790 |
| C26 | 0.1 | Polycarbonate | 100 | 20 | 943151 |
| C27 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C28 | | Not Used | | | |
| C29 | 39p | Mica | 350 | ±1p | 911243 |
| C30 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C31 | 39p | Mica | 350 | ±1p | 911243 |
| C32 | .01 | Ceramic | 50 | 20 | 938053 |
| C33 | 68p | Mica | 350 | 2 | 902230 |
| C34 | 100p | Mica | 500 | 5 | 943143 |
| C35 | 100p | Mica | 500 | 5 | 943143 |

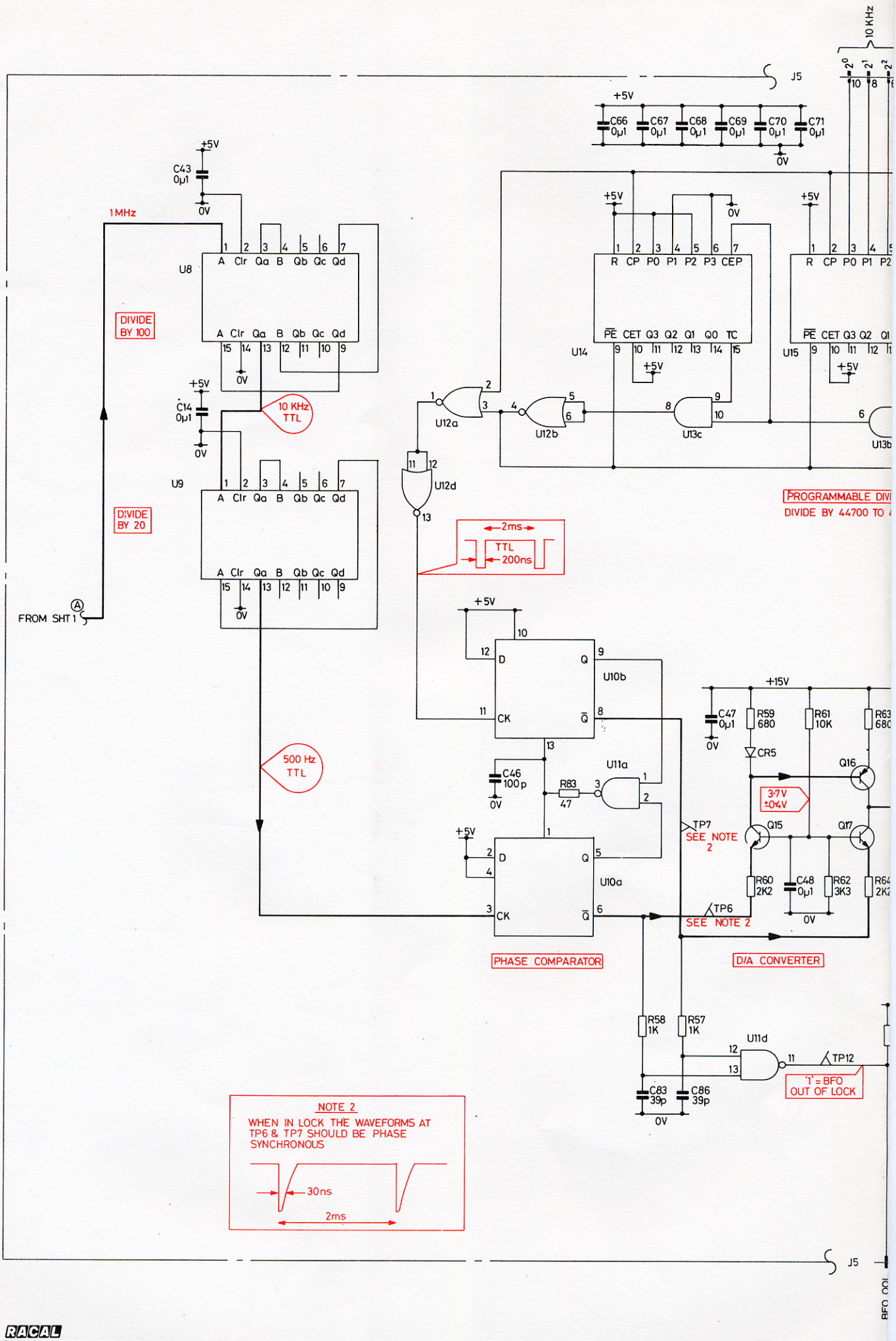
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Capacitors | | | V | | |
| C36 | 0.001 | Ceramic | 50 | 20 | 938408 |
| C37 | 100p | Mica | 500 | 5 | 943143 |
| C38 | 5p | Mica | 500 | ±½p | 943138 |
| C39 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C40 | 0.001 | Ceramic | 50 | 20 | 938408 |
| C41 | 68p | Mica | 350 | 2 | 902230 |
| C42 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C43 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C44 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C45 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C46 | 100p | Mica | 500 | 5 | 943143 |
| C47 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C48 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C49 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C50 | 0.47 | Polycarbonate | 100 | 20 | 918899 |
| C51 | 0.1 | Polycarbonate | 100 | 20 | 943151 |
| C52 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C53 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C54 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C55 | 56p | Mica | 50 | 5 | 940302 |
| C56 | 100p | Mica | 50 | 5 | 940305 |
| C57 | 100p | Mica | 500 | 5 | 943143 |
| C58 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C59 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C60 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C61 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C62 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C63 | 820p | Mica | 500 | 5 | 943145 |
| C64 | 150p | Mica | 350 | 2 | 902238 |
| C65 | 820p | Mica | 500 | 5 | 943145 |
| C66 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C67 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C68 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C69 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C70 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C71 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C72 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C73 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C74 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C75 | 0.1 | Ceramic | 50 | 20 | 938406 |

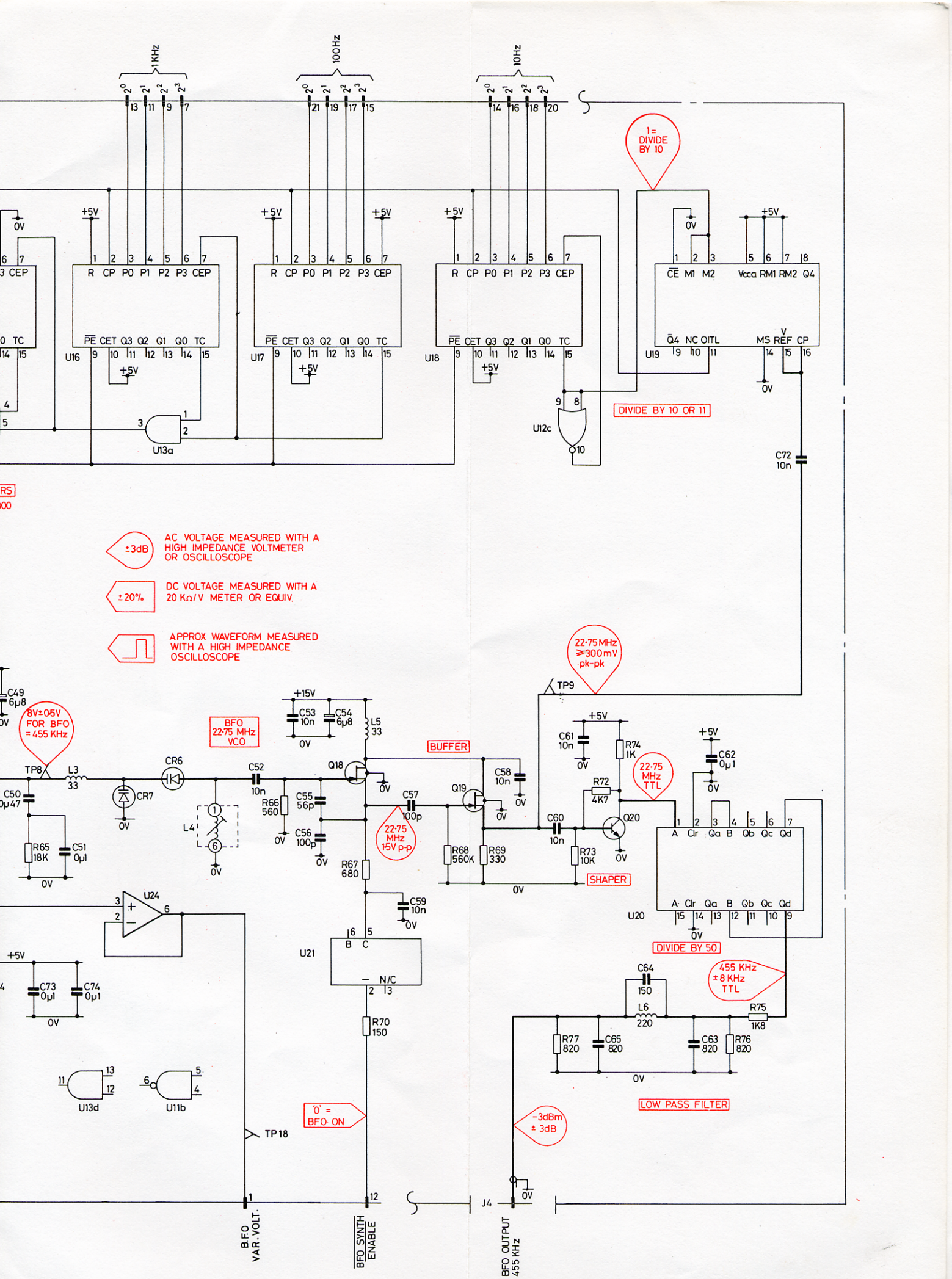
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Capacitors** | | | V | | |
| C76 | 82p | Mica | 350 | 2 | 902232 |
| C77 | 330p | Mica | 350 | 2 | 902246 |
| C78 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C79 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C80 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C81 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C82 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C83 | 39p | Mica | 350 | ±1p | 911243 |
| C84 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C85 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C86 | 39p | Mica | 350 | ±1p | 911243 |
| C87 | 0.001 | Ceramic | 50 | 20 | 938408 |
| * C88 | 3.3p | Mica | 100 | | 941162 |
| **Diodes** | | | | | |
| CR1 | | 1N4001 | | | 915266 |
| CR2 | | 1N916 | | | 913480 |
| CR3 | | 1N916 | | | 913480 |
| CR4 | | ZC706 | | | 920266 |
| CR5 | | 1N916 | | | 913480 |
| CR6 | | MV1650 | | | 915859 |
| CR7 | | MV1650 | | | 915859 |
| **Transistors** | | | | | |
| Q1 | | 2N2369 | | | 906842 |
| Q2 | | 2N2369 | | | 906842 |
| Q3 | | 2N2369 | | | 906842 |
| Q4 | | 2N2369 | | | 906842 |
| Q5 | | 2N2369 | | | 906842 |
| Q6 | | 2N2369 | | | 906842 |
| Q7 | | 2N3904 | | | 914046 |
| Q8 | | 2N4126 | | | 912678 |
| Q9 | | 2N3904 | | | 914046 |
| Q10 | | 2N2369 | | | 906842 |
| Q11 | | 2N2369 | | | 906842 |
| Q12 | | Not Used | | | |
| Q13 | | Not Used | | | |
| Q14 | | Not Used | | | |
| Q15 | | 2N3904 | | | 914046 |

* C88 is omitted if voltage at TP5 exceeds 10.5 V with C88 fitted.

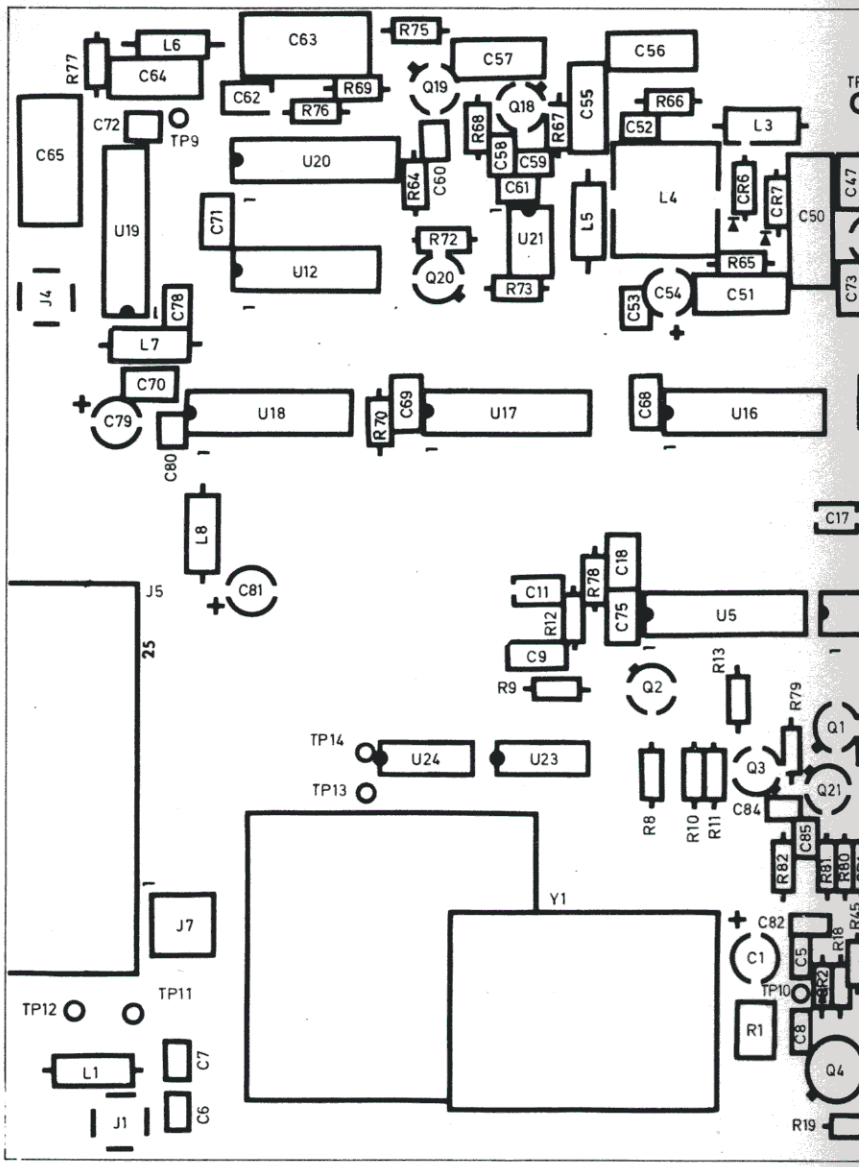
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Transistors** | | | | | |
| Q16 | | 2N4126 | | | 912678 |
| Q17 | | 2N3904 | | | 914046 |
| Q18 | | 2N3823 | | | 938592 |
| Q19 | | 2N3823 | | | 938592 |
| Q20 | | 2N2369 | | | 906842 |
| Q21 | | 2N2369 | | | 906842 |
| **Integrated Circuits** | | | | | |
| U1 | | 723PC Voltage Regulator | | | 925040 |
| U2 | | 74LS00 Quad 2-Input NAND gate | | | 939356 |
| U3 | | 74LS74 Dual D-type flip-flop | | | 939352 |
| U4 | | 74LS151 Data Selector Multiplex | | | 939355 |
| U5 | | 74LS151 Data Selector Multiplex | | | 939355 |
| U6 | | 74LS90 Decade Counter | | | 939358 |
| U7 | | 74LS74 Dual D-type flip-flop | | | 939352 |
| U8 | | 74LS390 Dual 4-bit decade | | | 939353 |
| U9 | | 74LS390 Dual 4-bit decade | | | 939353 |
| U10 | | 74LS74 Dual D-type flip-flop | | | 939352 |
| U11 | | 74LS00 Quad 2-Input NAND gate | | | 938598 |
| U12 | | 74LS02 Quad 2-Input NOR gate | | | 938531 |
| U13 | | 74LS08 Quad 2-Input AND gate | | | 939357 |
| U14 | | 74LS160 Synchronous 4-bit | | | 941992 |
| U15 | | 74LS160 Synchronous 4-bit | | | 941992 |
| U16 | | 74LS160 Synchronous 4-bit | | | 941992 |
| U17 | | 74LS160 Synchronous 4-bit | | | 941992 |
| U18 | | 74LS160 Synchronous 4-bit | | | 941992 |
| U19 | | 11C90 Pre-scaler | | | 938600 |
| U20 | | 74LS390 Dual 4-bit decade | | | 939353 |
| U21 | | 4N28 Opto-electronic coupler | | | 938601 |
| U22 | | 10115 - DC | | | 943285 |
| U23 | | CA 3140E Op. Amp. | | | 932204 |
| U24 | | CA 3140E Op. Amp. | | | 932204 |

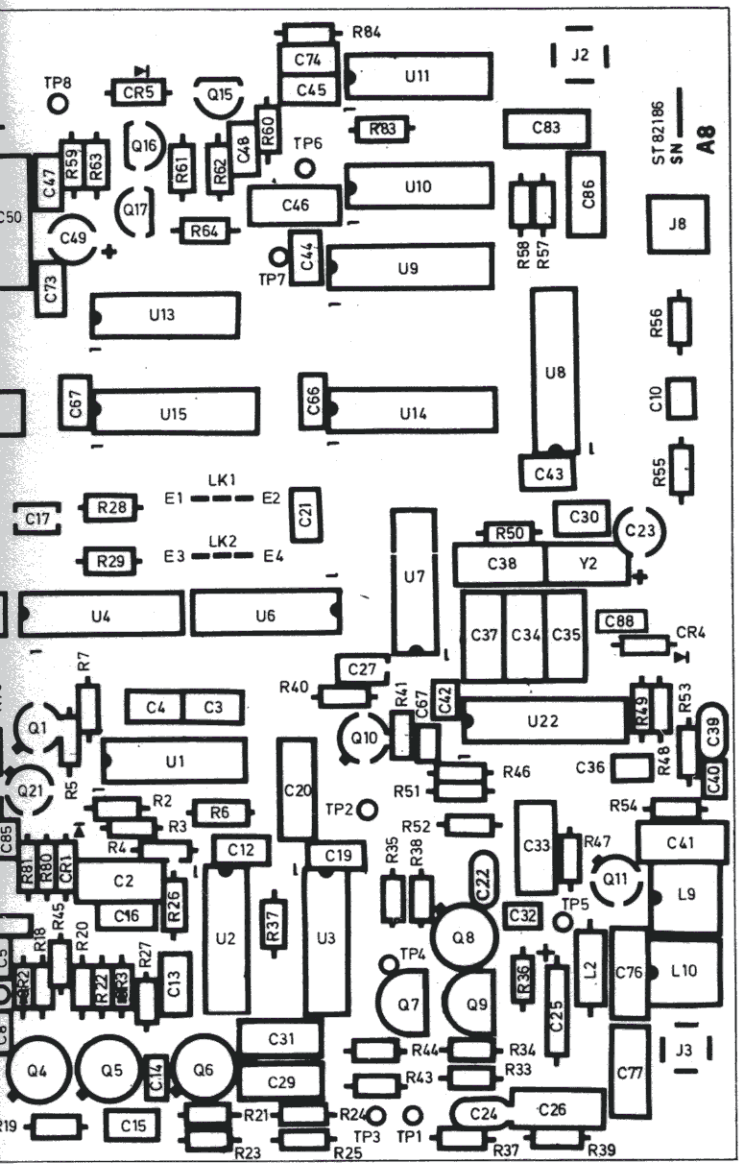
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Inductors** | | | | | |
| L1 | 100µ | Choke | | | 919471 |
| L2 | 1µ | Choke | | 10 | 915849 |
| L3 | 33µ | Choke | | | 919465 |
| L4 | | Choke, variable | | | AT81409 |
| L5 | 33µ | Choke | | | 919465 |
| L6 | 220µ | Choke | | | 918986 |
| L7 | 5.6µ | Choke | | | 922275 |
| L8 | 5.6µ | Choke | | | 922275 |
| L9 | | Choke, variable | | | AT81397 |
| L10 | | Choke, variable | | | AT81397 |
| **Connectors** | | | | | |
| J1 | | Plug, RF 50 ohms | | | 938429 |
| J2 | | Plug, RF 50 ohms | | | 938429 |
| J3 | | Plug, RF 50 ohms | | | 938429 |
| J4 | | Plug, RF 50 ohms | | | 938429 |
| J5 | | Plug, PCB Right angle 26-way | | | 938569 |
| J6 | | Connector Internal/External Select | | | B06846-2 |
| J7 | | Plug, RF 50 ohms | | | 938429 |
| J8 | | Plug, RF 50 ohms | | | 938429 |
| **Miscellaneous** | | | | | |
| Y2 | | Crystal 20,000 kHz | | | AD80547/1 |


10 KHz
J5
+5V
C66 0µ1
C67 0µ1
C68 0µ1
C69 0µ1
C70 0µ1
C71 0µ1
0V
C43 0µ1
1MHz
U8
A Clr Qa B Qb Qc Qd
DIVIDE BY 100
C14 0µ1
10 KHz TTL
U9
DIVIDE BY 20
FROM SHT 1
R CP P0 P1 P2 P3 CEP
PE CET Q3 Q2 Q1 Q0 TC
U14
U15
U12a
U12b
U13c
U13b
U12d
PROGRAMMABLE DIVI
DIVIDE BY 44700 TO
2ms
TTL
200ns
U10b
D Q CK
U10a
U11a
C46 100p
R83 47
500 Hz TTL
PHASE COMPARATOR
+15V
C47 0µ1
R59 680
R61 10K
R63 680
CR5
Q16
3·7V ±0·4V
Q15
Q17
TP7
SEE NOTE 2
R60 2K2
C48 0µ1
R62 3K3
TP6
SEE NOTE 2
D/A CONVERTER
R58 1K
R57 1K
U11d
TP12
'1' = BFO OUT OF LOCK
C83 39p
C86 39p
NOTE 2
WHEN IN LOCK THE WAVEFORMS AT TP6 & TP7 SHOULD BE PHASE SYNCHRONOUS
30ns
2ms
J5
BFO OUT




Circuit : 2nd L.O./B.F.O Synthesizer A8(Sheet 2) Fig.8.4


L6
C64
C63
R75
C57
C56
R77
C62
R69
Q19
R76
Q18
C55
R66
C72
TP9
R68
R67
C52
L3
C65
U20
C58
C59
C60
R64
C61
L4
CR6
CR7
C50
C47
U19
C71
U21
L5
R72
U12
Q20
R65
R73
C53
C54
C51
C73
J4
C78
L7
C70
C79
U18
R70
C69
U17
C68
U16
C80
C17
L8
C81
J5
C18
C11
R78
U5
R12
C75
25
C9
R13
R9
Q2
R79
Q1
TP14
U24
U23
Q3
Q21
TP13
C84
R8
R10
R11
C85
R82
R81
R80
Y1
J7
C82
C1
C5
R18
TP10
TP12
TP11
R1
C8
L1
C7
Q4
C6
J1
R19




Component Layout: 2nd L.O./B.F.O Synthesizer Fig.8.5

# CHAPTER 9

# FRONT PANEL SWITCH AND DISPLAY BOARD A9A1

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# CHAPTER 9

# FRONT PANEL SWITCH AND DISPLAY BOARD A9A1

## INTRODUCTION

1. This board is mounted on the inner face of the front sub-panel and accommodates the two liquid-crystal display panels with associated drivers, the front panel pushbutton switches, and a number of through connections between the front panel memory board and the PHONES jack, loudspeaker, VOLUME control, IF GAIN control and METER switch on the front panel.

## CIRCUIT DESCRIPTION (Fig. 9.1)

### Switch Matrix

2. The front-panel, spring-loaded, single make-contact pushbutton switches are connected as a four-column (A,B,C,D) by eight-row (0 to 7) matrix which is continually read by the microcomputer via additional circuitry located on the front panel memory board (Chapter 10).

### Display Oscillator

3. The liquid crystal display driver devices (U3 to U26 and U28) require a low-frequency squarewave input signal. This signal is produced by U29 which is connected as an astable multivibrator and runs at a nominal frequency of 125 Hz (timing components R2, C2). The Q output signal is connected in parallel to the DF (display frequency) input pin of each driver device, whilst the $\overline{Q}$ output is routed to the front panel memory board where it is used to generate a -30 V supply for the EAROM devices (Chapter 10).

### Number Displays

4. The number displays i.e. the frequency, channel number, BFO frequency and bandwidth displays, are all driven by a number of BCD to 7-segment C-MOS drivers U5, U6, U10 to U20, U24 and U25. These devices decode the applied 1-2-4-8 BCD input signals to provide the required 7-segment output signals which are produced at the a to g output pins when a positive voltage is applied to the strobe input. When a '0' is present at the strobe input, the data is latched at the a to g output pins.

5. The strobe signals for the 7-segment display drivers are produced by U27 which consists of a 4-bit latch and a 4-line to 16-line decoder. A '1' is applied to the inhibit input to set all the strobe outputs to a '0' whilst the binary number display address at the A,B,C and D input pins is latched. The inhibit input is then pulsed to a '0' to produce the required positive-going output strobe pulse.

Non-numerical Displays

6. The remaining (non-numerical) displays are driven by a number of 4-segment C-MOS drivers U3, U4, U7, U8, U9, U21, U22, U23, U26 and U28. These devices are similar in operation to the 7-segment devices except that individual strobe inputs are provided for each segment. In this application, however, the four strobe inputs of each device are commoned except for U28 where strobe 4 is permanently connected to the +5 V rail to connect the common and unused pins of the two display panels to 0 V. The remaining strobe signals are produced on the front panel memory board (Chapter 10).

## FRONT PANEL SWITCH AND DISPLAY BOARD (ST 08198)

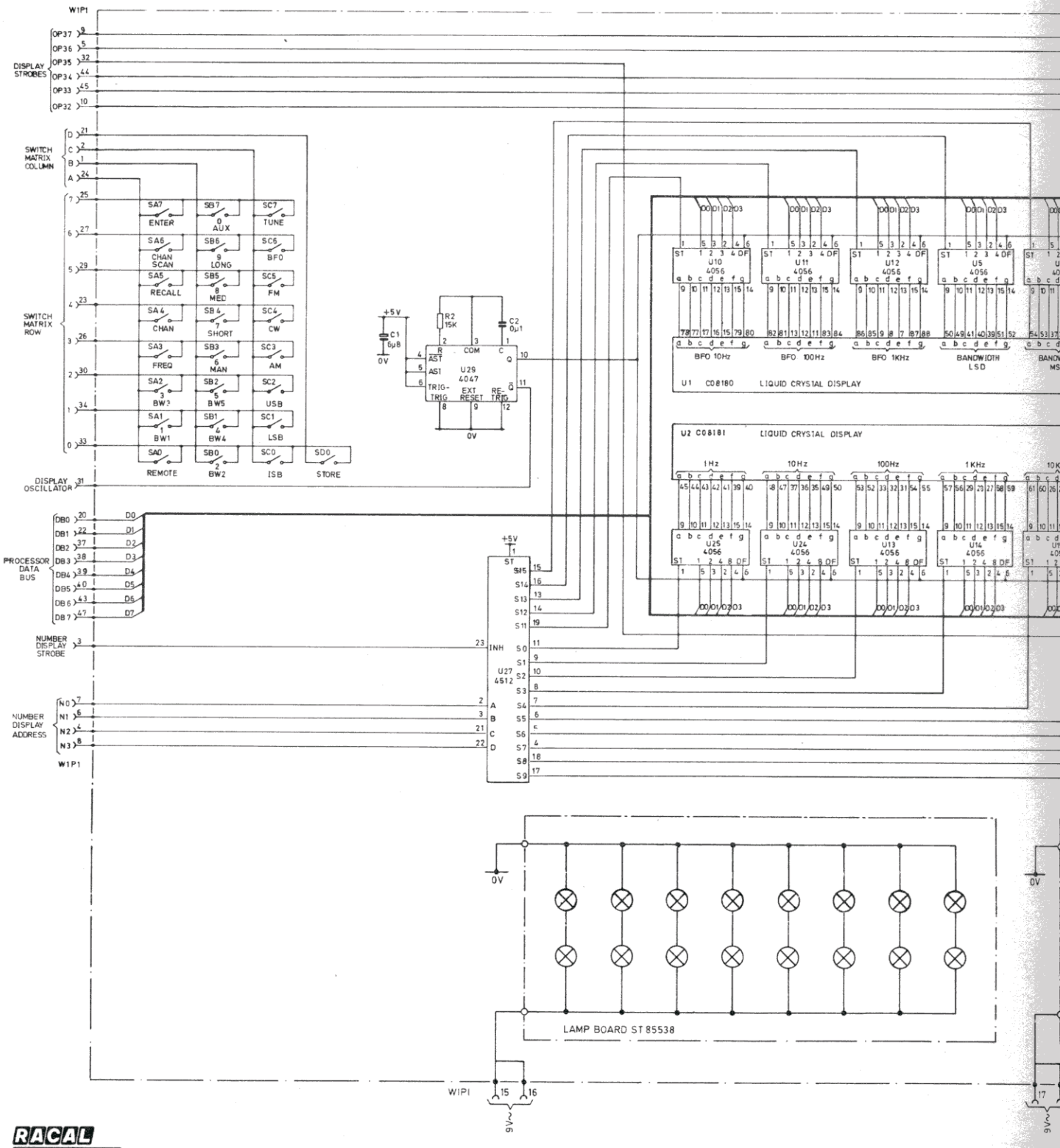
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R1 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R2 | 15k | Metal Oxide | ¼ | 2 | 920645 |
| R3 | 15k | Metal Oxide | ¼ | 2 | 920645 |
| R4 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| **Capacitors** | | | | | |
| C1 | 6µ8 | Tantalum | 35 | 20 | 938030 |
| C2 | 100n | Ceramic | 50 | 20 | 938406 |
| C3 | 6µ8 | Tantalum | 35 | 20 | 938030 |
| C4 | 6µ8 | Tantalum | 35 | 20 | 938030 |
| **Switches** | | | | | |
| SA0 to SD0 | | Pushbutton | | | 938467 |

### Switch Keytops

| Keytop | Part No. | Keytop | Part No. | Keytop | Part No. |
|---|---|---|---|---|---|
| ENTER | BD81103/36 | STORE | BD81103/58 | 6/MAN | BD81103/67 |
| AM | BD81103/45 | ISB | BD81103/59 | 7/SHORT | BD81103/68 |
| FM | BD81103/46 | LSB | BD81103/60 | 8/MED | BD81103/69 |
| CW | BD81103/47 | USB | BD81103/61 | 9/LONG | BD81103/70 |
| CHAN | BD81103/53 | 1/BW | BD81103/62 | 0/AUX | BD81103/71 |
| RCL | BD81103/54 | 2/BW2 | BD81103/63 | FREQ. | BD81103/79 |
| TUNE | BD81103/55 | 3/BW3 | BD81103/64 | CHAN SCAN | BD81103/80 |
| BFO | BD81103/56 | 4/BW4 | BD81103/65 | | |
| REM | BD81103/57 | 5/BW5 | BD81103/66 | | |

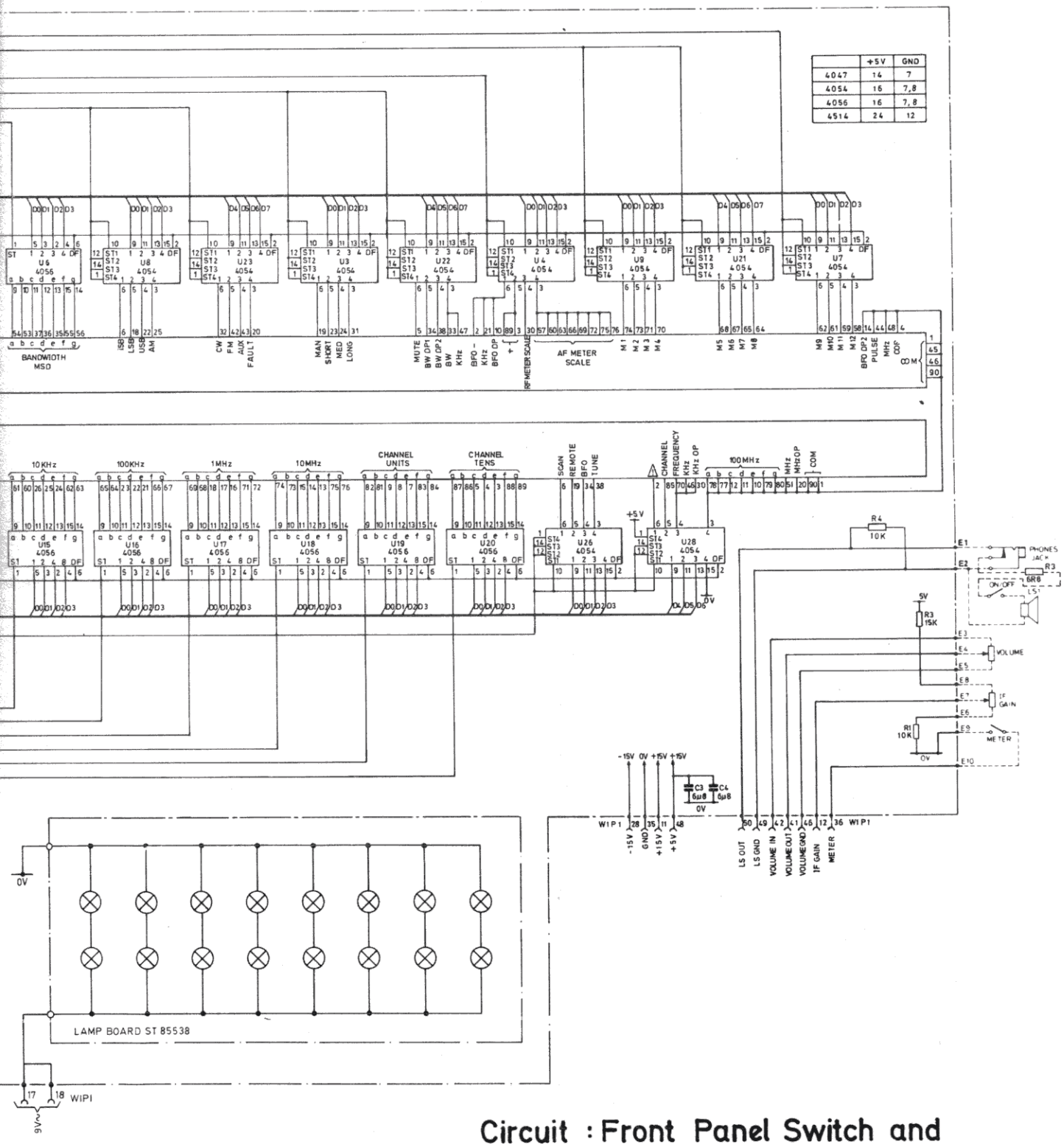
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Connectors** | | | | | |
| W1 | | Cable Assembly | | | B08290 |
| | | Comprising: | | | |
| | | Connector, PCB, 50-way | | | 927270 |
| | | Cable, flat, 50-way | | | 927301 |
| | | Socket, 50-way | | | 934413 |
| | | Clamp, Strain Relief | | | 934414 |
| **Integrated Circuits** | | | | | |
| U1 | | Liquid Crystal Display Mode | | | CD84311 |
| U2 | | Liquid Crystal Display Frequency | | | CD84310 |
| U3 | | LCD Driver 4054 | | | 938464 |
| U4 | | LCD Driver 4054 | | | 938464 |
| U5 | | LCD Driver 4056 | | | 938465 |
| U6 | | LCD Driver 4056 | | | 938465 |
| U7 | | LCD Driver 4054 | | | 938464 |
| U8 | | LCD Driver 4054 | | | 938464 |
| U9 | | LCD Driver 4054 | | | 938464 |
| U10 | | LCD Driver 4056 | | | 938465 |
| U11 | | LCD Driver 4056 | | | 938465 |
| U12 | | LCD Driver 4056 | | | 938465 |
| U13 | | LCD Driver 4056 | | | 938465 |
| U14 | | LCD Driver 4056 | | | 938465 |
| U15 | | LCD Driver 4056 | | | 938465 |
| U16 | | LCD Driver 4056 | | | 938465 |
| U17 | | LCD Driver 4056 | | | 938465 |
| U18 | | LCD Driver 4056 | | | 938465 |
| U19 | | LCD Driver 4056 | | | 938465 |
| U20 | | LCD Driver 4056 | | | 938465 |
| U21 | | LCD Driver 4054 | | | 938464 |
| U22 | | LCD Driver 4054 | | | 938464 |
| U23 | | LCD Driver 4054 | | | 938464 |
| U24 | | LCD Driver 4056 | | | 938465 |
| U25 | | LCD Driver 4056 | | | 938465 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| U26 | | LCD Driver 4054 | | | 938464 |
| U27 | | 4-bit latch/1 of 16 decoder 4514 | | | 931010 |
| U28 | | LCD Driver 4054 | | | 938464 |
| U29 | | Multivibrator 4047 | | | 936622 |
| | | | | | |
| Miscellaneous | | | | | |
| | | 14-pin DIL IC Socket | | | 930605 |
| | | 16-pin DIL IC Socket | | | 930606 |
| | | 24-pin DIL IC Socket | | | 928024 |
| | | | | | |
| | | LAMP BOARD ST 85538 | | | |
| | | Lamp 5 V 0.3 W | | | 941840 |

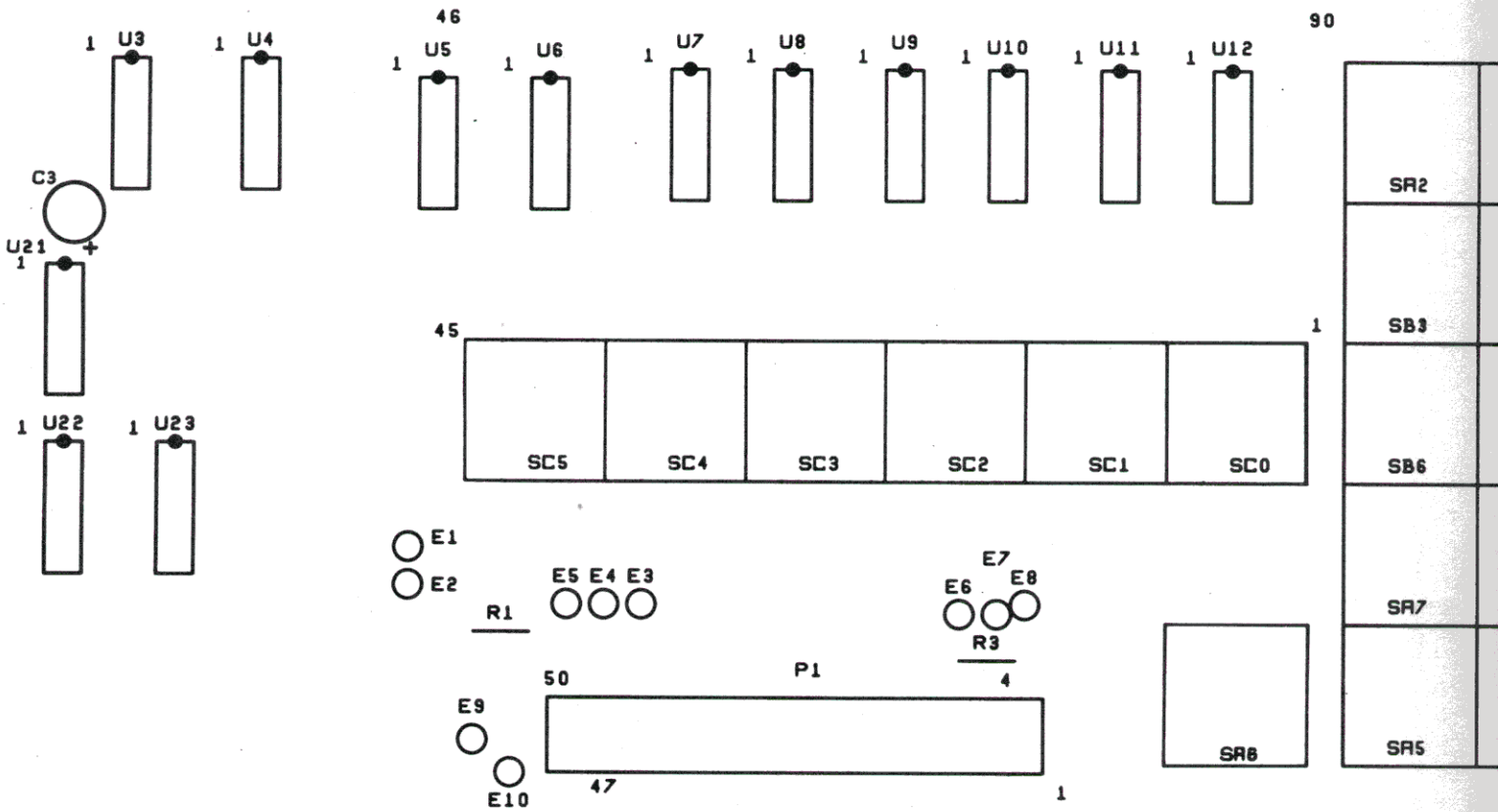



RACAL

| TH3416 | DC08197 |
|---|---|
| 3 4 5 | |

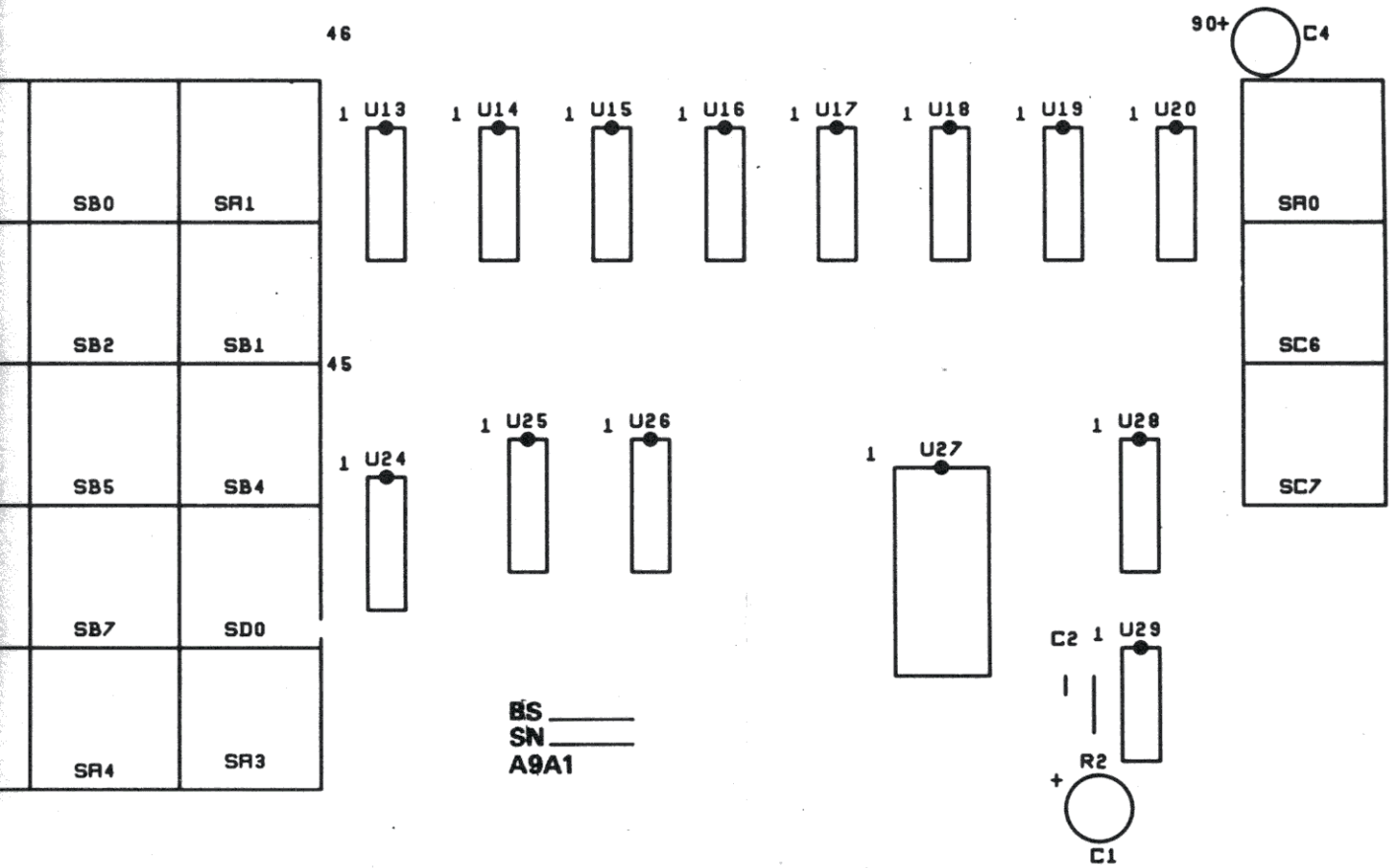



**Circuit : Front Panel Switch and Display Board A9A1** **Fig. 9.1**




RACAL

| TH3416 | EA80781 |
|---|---|
| 4 | 9 |




Component Layout : Front Panel
Switch and Display Board Fig.9.2

# CHAPTER 10

# FRONT PANEL MEMORY BOARD A9A2

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# CHAPTER 10

# FRONT PANEL MEMORY BOARD

## INTRODUCTION

1. The front panel memory board forms the interface between the microcomputer and the front panel switch and display board, and the audio board. It also contains the tuning control shaft encoder and an electrically alterable read-only memory (EAROM) which is used to store channel information.

## CIRCUIT DESCRIPTION (Fig.10.1)

### Switch Matrix Interface

2. The pushbutton switches on the front panel switch and display board (Chapter 9) are connected as a four-column (A,B,C,D) by eight row (0 to 7) matrix. The microcomputer causes the application of a 0 V signal, in turn, to each column line, and the 0 V signal resulting from a depressed pushbutton is routed to the microcomputer via the I/O data bus. The action of the circuit is as follows.

3. U10 is connected as an 8-channel demultiplexer; when a '0' is present at the inhibit input (device enabled), the input signal at the X input is routed to one of the eight outputs (0 to 7), as selected by the binary levels at the A, B and C input pins. When addresses in the range hexadecimal 20 to 23 are applied to the IOC bus (table 1), together with a '0' at the /IO READ input, the following conditions arise:

   (1) The '1' at the IOC5 line is inverted by NOR gate U7a, and the inhibit condition is removed from U10.

   (2) The '0' at the IOC2 line is applied to the C input of U10, whilst the levels on IOC0 and IOC1 lines are applied to the A and B inputs respectively of U10 to route the '0' at the X input (/IO READ signal) to the 0, 1, 2 or 3 output.

   (3) The '0' at the IOC2 line is gated (U7c) with the '0' at the /IO READ line to produce a '1' at the output; this is gated with the '1' at the IOC5 line to produce a '0' at the output of U6a, and this is used to enable tri-state buffers U16b, U17a for the switch matrix row input data.

### EAROM Addressing

4. The two 1 k by 4-bit EAROM devices U13, U14, are connected as a 1 k by 8-bit memory, where the low order nibble is stored in U13 and the high order nibble is stored in U14. To address the EAROM, the microcomputer applies hexadecimal address 31 to the IOC bus i.e. IOC5, IOC4 and IOC0 lines at '1', remainder at '0', together with the three least significant bits of

the EAROM address (A2, A1, A0) to the IOD bus, lines IOD2, IOD1 and IOD0 respectively. With the IOC4 and IOC5 lines both at '1', a '0' is produced at the output of NAND gate U6d, and this is applied to one input of NOR gate U7b. Provided the write strobe (/WSTB) signal, which is applied to the remaining input of U7b, is at a '0', then a '1' is produced at the output of U7b, which is applied to the trigger input of a pulse generator U9a, U9b.

This dual monostable produces a delayed and extended negative-going output pulse which is applied to the inhibit input (to remove the inhibit condition) of a 4-bit latch/4-line to 16-line decoder U8.

Table 1: Switch Matrix Interface

| INPUT PORT (IOC BUS) | | IO | SWITCH MATRIX | | |
|---|---|---|---|---|---|
| HEX | 7 6 5 4 3 2 1 0 | READ | COLUMN | ROW | CONTENT |
| 20 | 0 0 1 0 0 0 0 0 | | A | 0 | REMOTE |
| | | | | 1 | 1, BW1 |
| | | | | 2 | 3, BW3 |
| | | | | 3 | FREQ |
| | | | | 4 | CHAN |
| | | | | 5 | RECALL |
| | | | | 6 | CHAN SCAN |
| | | | | 7 | ENTER |
| 21 | 0 0 1 0 0 0 0 1 | | B | 0 | 2, BW2 |
| | | | | 1 | 4, BW4 |
| | | | | 2 | 5, BW5 |
| | | | | 3 | 6, MAN |
| | | | | 4 | 7, SHORT |
| | | | | 5 | 8, MED |
| | | | | 6 | 9, LONG |
| | | | | 7 | 0, AUX |
| 22 | 0 0 1 0 0 0 1 0 | | C | 0 | ISB |
| | | | | 1 | LSB |
| | | | | 2 | USB |
| | | | | 3 | AM |
| | | | | 4 | CW |
| | | | | 5 | FM |
| | | | | 6 | BFO |
| | | | | 7 | TUNE |
| 23 | 0 0 1 0 0 0 1 1 | | D | 0 | STORE |
| | | | | 1-7 | NOT USED |

5. The '1' at the IOC5 line is also used to enable transmission gate U3a which routes the '0' write strobe signal to the negative-edge triggered quad D-type latches U19 and U20. The three least significant bits of the EAROM address at the D1, D4 and D2 inputs of U19 are then latched at the respective Q outputs and applied to data bus lines DB0, DB1 and DB2 respectively.

6. Thus with hex.31 present on the IOC bus and the write strobe signal at '0', a '1' is present at the strobe input of U8 (Q4 held off), a '1' is also present at the A input, and a '1' is produced at the S1 output for the duration of the negative-going output pulse from U9b. The binary up-counter U12 (up/down input connected to +5 V) is preset-enabled, and the three least significant bits of the EAROM address at the Q1, Q2 and Q3 outputs are applied to the A0, A1 and A2 inputs of the two EAROM devices.

7. Hexadecimal 20 is then applied to the IOC bus (IOC5 at '1', remainder at '0') to route the most significant bits (A3 to A9) of the required EAROM address to the EAROM devices via the IOD data bus (IOD0 to IOD6). The '1' at the IOC5 line enables U3a, the '0' write strobe signal clocks U19 and U20, and the seven bits of the address are applied to the EAROM devices via data bus lines DB0 to DB6.

EAROM Mode Control

8. Each EAROM device has an active-low chip enable ($\overline{CE}$) input, an active-low write enable ($\overline{WE}$) input, and two mode control inputs, C0 and C1. The code set on the two mode control lines (table 2) is latched into the device on the negative-going edge of the $\overline{CE}$ signal. When in the read mode data is read during each $\overline{ES}$ pulse. Writing or erasing continues for as long as the device is latched in the write or erase mode. Consequently the software responds with a series of commands to terminate a write cycle by effecting a dummy read cycle. The word erase cycle erases one 4-bit word in each device whilst the block erase mode (not used in this application) erases the complete memory.

Table 2: EAROM Mode Control

| C1 | C0 | MODE |
|---|---|---|
| 0 | 0 | READ |
| 0 | 1 | WRITE |
| 1 | 0 | BLOCK ERASE |
| 1 | 1 | WORD ERASE |

EAROM Read Cycle

9. To read data from the EAROM the address is first set up (para.4) and hexadecimal 24 is then applied to the IOC bus (IOC5 and IOC2 at '1', remainder at '0'). The '1' at the IOC5 line is inverted by U7a to remove the inhibit condition from U10, whilst the '1' at the IOC2 line routes the '0' IO read pulse at the X input of U10 to the 4 output. The EAROM devices are enabled and the stored byte of data at the addressed location is applied to the microcomputer via the IOD bus. At the end of the read cycle, the EAROM $\overline{CE}$ input returns to a '1', and this is also used to clock the binary up-counter U12 via AND gate U5b to increment the EAROM address. Thus once the initial EAROM address has been established, eight successive bytes of EAROM data may be read by applying hex.24 to the IOC bus eight times in succession (one stored channel constitutes eight bytes of EAROM data).

EAROM Write Cycle

10. To write data into the EAROM, the addressed byte is first erased, the erase cycle is terminated by a dummy read cycle, and the write cycle is then commenced. The write cycle is also terminated by a dummy read cycle. To set the EAROM to the erase mode, hexadecimal 43 is applied to the IOC bus (table 3). The $\overline{IO}$ read line is then pulsed to '0' with the following result.

(1) The '0' at the $\overline{IO}$ read line is inverted by U7d and is then gated with the '1' at the IOC6 line (AND gate U5a) to set D-type flip-flop U4a. The resulting '1' at the $\overline{Q}$ output enables transmission gate U3b and a '0' is applied to the $\overline{CE}$ inputs of the two EAROM devices.

Table 3: EAROM Write Cycle

| | INPUT PORT | | |
|---|---|---|---|
| HEX | 7 6 5 4 | 3 2 1 0 | FUNCTION |
| 43 | 0 1 0 0 | 0 0 1 1 | ERASE |
| 24 | 0 0 1 0 | 0 1 0 0 | DUMMY READ |
| 41 | 0 1 0 0 | 0 0 0 1 | WRITE |
| 24 | 0 0 1 0 | 0 1 0 0 | DUMMY READ |

(2) The '1-1' code at IOC lines 0 and 1 is latched into the EAROM devices to select the erase mode.

11. The write strobe line is then pulsed to '0'. This is routed to the EAROM write enable input, and the addressed EAROM byte is erased. The rising edge of the write enable pulse then clocks U4a, the '0' at the D input is transferred to the Q output, U3b is disabled, and the '0' is removed from the EAROM chip enable ($\overline{CE}$) input.

12. The rising edge of the chip enable pulse is applied to the clock input of up-counter U12 via AND gate U5b (the remaining input to U5b is also at a '1'; with U8 in the inhibit condition, the S outputs are all at '0', and the output of inverting NAND gate U6b is thus at logic '1'). The EAROM address is incremented in readiness for the dummy read cycle, which is initiated by the application of hex. 24 to the IOC bus and a '0' pulse to the IO read line (para.9). Following the dummy read cycle, the EAROM write address is re-established by the application of hex.31 followed by hex. 20 to the IOC bus (para.4).

13. To set the EAROM to the write mode, hex. 41 is applied to the IOC bus (table 3). The IO read line is pulsed to a '0', U4a is set, and a '0' pulse is applied to the EAROM chip enable input to latch the '1-0' code at the C0 and C1 input pins into the EAROM devices. The write strobe line is then pulsed, the EAROM is write-enabled, and the byte of data at the IOD bus is written into the addressed EAROM location. Finally, a further dummy read operation (hex. 24 at the IOC bus) is performed to terminate the write cycle.

-30 V Generator

14. In addition to the +5 V VSS supply and the -12 V VDD supply (from 3-terminal regulator U11), the EAROM devices require a -30 V supply (VGG). This is derived from the nominal 125 Hz square-wave output signal produced by the display oscillator on the front panel switch and display board, connected to J2 pin 31. During the negative-going excursion of the 125 Hz square wave signal, Q1 conducts and Q2 is held off. C7 therefore charges to approximately 20 V (from -15 V supply via CR3 and via CR1, Q1 and R27 to +5 V), whilst C8 charges to approximately -15 V (via CR2). During the positive-going excursion of the 125 Hz square wave signal, Q1 is cut off, allowing Q2 to conduct. The emitter of Q2 is pulled down to approximately -15 V, and C7 pumps current into C8 via CR4. C8 thus attempts to charge to approximately -35 V but R3 and 30 V zener diode CR5 limit the output to the required -30 V. C6 is included to prevent switching spikes reaching the +5 V supply.

Optical Shaft Encoder

15. The front panel tuning-control is mechanically linked to an optical shaft encoder which may be used to set the receiver operating frequency, the BFO frequency, or to display the parameters of a particular channel (manual scan mode). A polished metal disc with radial black stripes is attached to the tuning control spindle, and is made to rotate over a pair of reflective optical switches, each consisting of a light emitting diode (LED) and a photo-transistor. As the disc rotates, the photo-transistors are alternately illuminated and darkened resulting in two alternating output waveforms. The optical switches are physically displaced such that these two waveforms, A and B, are 90 degrees out of phase, with output A leading output B for one direction of rotation, and lagging output B for the opposite direction of rotation.

16. U28a and U28b are connected as Schmidt triggers to square-up the output waveforms (feedback components R12, C14 and R13, C15); these are fed to the microcomputer, via IOD bus lines IOD0 and IOD1, where they are counted by a software counter. U17b is enabled by the application of hex. 25 to the IOC bus; the resulting '0' at the 5 output of U10 also enables U15 to route miscellaneous data from the audio board to the microcomputer via IOD bus lines IOD2 to IOD7 (table 4).

17. As the turning rate of the the tuning control is varied, so the count read on bits 0 & 1 varies (see table 4). This causes the microcomputer to raise or lower the rate of frequency change as the tuning shaft is rotated faster or slower. The rate of frequency change varies from 1 kHz per turn to approximately 20 kHz per turn, depending upon the speed of rotation.

Table 4: Miscellaneous Read Data 1

| INPUT PORT | | | IO READ | |
|---|---|---|---|---|
| HEX | 7 6 5 4 | 3 2 1 0 | BIT | DATA |
| 25 | 0 0 1 0 | 0 1 0 1 | 0 | Shaft Encoder |
| | | | 1 | Data |
| | | | 2 | AF Comparator |
| | | | 3 | IF Comparator |
| | | | 4 | Set Check |
| | | | 5 | Meter Switch |
| | | | 6 | Mute |
| | | | 7 | Scan Inhibit |

Miscellaneous Read Data 2

18. The microcomputer applies hexadecimal 26 to the IOC bus to enable U16a and U18 ('0' at 6 output of U10). The resulting data applied to the IOD bus is listed in table 5.

Table 5: Miscellaneous Read Data 2

| INPUT PORT | | | IO READ | |
|---|---|---|---|---|
| HEX | 7 6 5 4 | 3 2 1 0 | BIT | DATA |
| 26 | 0 0 1 0 | 0 1 1 0 | 0 | S1b Fault Analysis |
| | | | 1 | Not used |
| | | | 2 | S1a Preset mode |
| | | | 3 | Spare |
| | | | 4 | Not used |
| | | | 5 | S1c ISB Fitted |
| | | | 6 | Word Present |
| | | | 7 | New Data |

Numeric Display Data

19. The numeric display data, i.e. frequency, channel number, BFO frequency and bandwidth display data, is routed to the front panel switch and display board from the microcomputer via the IOD bus and the front panel memory board. Circuitry on the front panel memory board also produces the number display strobe and the number display address.

20. Hexadecimal 31 is applied to the IOC bus to initially set the number display address in readiness for the next numerical display update routine. The '1' at the IOC5 line enables U3a for the write strobe ($\overline{\text{WSTB}}$) signal, the negative-going edge of which clocks U19 to transfer hex. zero at IOD bus lines 0 to 3 to the parallel inputs P1 to P4 of the up-counter U12. The '1' at the IOC5 line is also applied to NAND gate U6d where it is combined with the '1' at the IOC4 line to produce a '0' at the output. This is combined with the negative-going write strobe signal (NOR gate U7b) to produce a '1' at the trigger (A) input of the pulse generator U9a, U9b. The negative-going output pulse removes the inhibit condition from U8, and since both the A and strobe inputs are both at '1' (A input from the IOC1 line, strobe input from the collector of non-conducting transistor Q4), a positive-going pulse is produced at the S1 output. This is applied to the preset-enable (PE) input of up-counter U12, and the zero code at the parallel inputs is transferred via the Q outputs as the number display address to the front panel switch and memory board.

21. Hexadecimal 30 is then applied to the IOC bus coincident with the 7-segment BCD data for the 10 Hz frequency digit, which is applied to the IOD bus (lines 0 to 3). The '1' at the IOC5 line together with the negative-going write strobe signal transfers the 10 Hz frequency digit data to the front panel switch and display board via U19 and data bus lines DB0 to DB3, whilst the combination of the '1' at the IOC5 line, the '1' at the IOC4 line, and the write strobe signal produces a positive going pulse at the S0 output of U8 (A,B,C and D inputs all at '0'). This is inverted by NAND gate U6b, a negative-going number display strobe pulse is produced, and the 10 Hz frequency digit data is loaded into the appropriate LCD driver stage on the front panel switch and display board.

22. The positive-going edge of the negative-going pulse from U6b is applied via AND gate U5b to the clock input of up-counter U12, which then increments the number display address. Hexadecimal 30 is then repeatedly applied to the IOC bus to update, in turn, the remaining numeric displays, as listed in table 6.

Table 6: Numeric Display Data

| NUMBER DISPLAY ADDRESS | | | | | DATA BUS (DB0 to DB3) |
|---|---|---|---|---|---|
| HEX | N3 | N2 | N1 | N0 | |
| 1 | 0 | 0 | 0 | 1 | 10 Hz |
| 2 | 0 | 0 | 1 | 0 | 100 Hz — OPERATING |
| 3 | 0 | 0 | 1 | 1 | 1 kHz — FREQUENCY |
| 4 | 0 | 1 | 0 | 0 | 10 kHz — DISPLAY |
| 5 | 0 | 1 | 0 | 1 | 100 kHz — DATA |
| 6 | 0 | 1 | 1 | 0 | 1 MHz |
| 7 | 0 | 1 | 1 | 1 | 10 MHz |
| 8 | 1 | 0 | 0 | 0 | CHANNEL NUMBER LS DIGIT |
| 9 | 1 | 0 | 0 | 1 | CHANNEL NUMBER MS DIGIT |
| A | 1 | 0 | 1 | 0 | NOT USED |
| B | 1 | 0 | 1 | 1 | 10 Hz |
| C | 1 | 1 | 0 | 0 | 100 Hz — BFO FREQUENCY DATA |
| D | 1 | 1 | 0 | 1 | 1 kHz |
| E | 1 | 1 | 1 | 0 | BANDWIDTH LS DIGIT |
| F | 1 | 1 | 1 | 1 | BANDWIDTH MS DIGIT |

Non-Numeric Display Data

23. The strobe signals for the non-numeric display drivers on the front panel switch and display board are produced at the S2 to S7 output pins of U8, in response to IOC bus output port addresses 32 to 37 respectively. For each of these addresses, the combination of the '1' at the IOC5 line and the negative-going write strobe signal transfers the display data from the IOD bus to the DB bus via U19 and U20, whilst the combination of the '1' at the IOC5 line, the '1' at the IOC 4 line and the write strobe signal removes the inhibit from, and applies the strobe to, U8. The levels at the IOC0 to IOC3 lines are then decoded to produce the required output strobe signal (table 7).

## Table 7: Non-Numeric Display Data

| IOC BUS | | | DISPLAY DATA | |
|---|---|---|---|---|
| HEX | 7 6 5 4 | 3 2 1 0 | BIT NO. | DATA |
| 32 | 0 0 1 1 | 0 0 1 0 | 0 | ISB |
| | | | 1 | LSB |
| | | | 2 | USB |
| | | | 3 | AM |
| | | | 4 | CW |
| | | | 5 | FM |
| | | | 6 | AUX |
| | | | 7 | FAULT |
| 33 | 0 0 1 1 | 0 0 1 1 | 0 | MAN |
| | | | 1 | SHORT |
| | | | 2 | MED |
| | | | 3 | LONG |
| | | | 4 | MUTE |
| | | | 5 | BANDWIDTH DP1 (RH) |
| | | | 6 | BANDWIDTH DP2 (LH) |
| | | | 7 | BANDWIDTH kHz |
| 34 | 0 0 1 1 | 0 1 0 0 | 0 | BFO-, kHz. BFO DP |
| | | | 1 | BFO + |
| | | | 2 | RF METER SCALE |
| | | | 3 | AF METER SCALE |
| | | | 4 - 7 | NOT USED |
| 35 | 0 0 1 1 | 0 1 0 1 | 0 | SCAN |
| | | | 1 | REMOTE |
| | | | 2 | BFO |
| | | | 3 | TUNE |
| | | | 4 | ! |
| | | | 5 | CHANNEL |
| | | | 6 | FREQUENCY |
| | | | 7 | kHz and dp |
| 36 | 0 0 1 1 | 0 1 1 0 | 0 | M1 |
| | | | 1 | M2 |
| | | | 2 | M3 METER READING |
| | | | 3 | M4 10(-9) to 8(-2) |
| | | | 4 | M5 |
| | | | 5 | M6 |
| | | | 6 | M7 |
| | | | 7 | M8 |
| 37 | 0 0 1 1 | 0 1 1 1 | 0 | M9 |
| | | | 1 | M10 METER READING |
| | | | 2 | M11 90(-1) to 120 (+2) |
| | | | 3 | M12 |

24. U8 outputs are used as strobes to various areas in the RA 1792 Receiver and consist of a positive-going 1 µs pulse. Table 8 lists the output, appropriate address and destination of each U8 strobe.

Table 8: U8 Outputs

| OUTPUT | IOC BUS ADDRESS (HEX) | STROBE FOR: |
|---|---|---|
| S0 | OP 30 | NUMERIC DISPLAY & COUNTER INCREMENT |
| S1 | OP 31 | DISPLAY PRESET & SYNTHESIZER |
| S2 | OP 32 | DISPLAY LATCHES |
| S3 | OP 33 | |
| S4 | OP 34 | |
| S5 | OP 35 | |
| S6 | OP 36 | |
| S7 | OP 37 | |
| S8 | OP 38 | BFO LATCH |
| S9 | OP 39 | SYNTHESIZER LATCH |
| S10 | OP 3A | ISB IF |
| S11 | OP 3B | NOT USED |
| S12 | OP 3C | MAIN IF |
| S13 | OP 3D | AUXILIARY IF |
| S14 | OP 3E | DIGITAL TO ANALOGUE CONVERTER |
| S15 | OF 3F | AUDIO CROSSPOINT SWITCH |

## BITE

### Voltage Measurements

25. The section of BITE (Built in Test Equipment) which is housed on the Front Panel Memory Board, measures receiver DC Power Supply voltages, plus A3 AGC voltage. Also, loop out-of-lock (OOL) voltages, Reference, BFO and Synthesizer may be selected by links 3, 4 and 5 respectively.

Circuit Operation

26. U31 is a 1 of 16 analogue multiplexer. Voltages to be measured after suitable conditioning, are applied to 11 of the 16 possible inputs, the remaining 5 being grounded. The voltage to be measured is selected by the binary code applied to pins 10, 11, 13, 14 from U32, a TTL to CMOS level-shifter.

27. U12, a counter, may be preset to any required state by D0, D1, D2 and D3 of the microcomputer data bus. Data is preset by the OP 31 strobe from U8 (see Para 24 & table 9), and U12 is clocked by OP 30 strobe, via U6b and U5b. U12 Q outputs are applied to U32, which after level shifting selects the voltage to be measured by selection of the appropriate U31 input. Table 10 lists the voltage measurements made by BITE via U31.

Table 9: BITE Voltage Measurement

| Voltage | N0 | N1 | N2 | N3 | Remarks |
|---|---|---|---|---|---|
| +5 V | 0 | 0 | 0 | 0 | |
| -12 V | 0 | 0 | 0 | 1 | |
| +20 V | 0 | 0 | 1 | 0 | |
| +15 V | 0 | 0 | 1 | 1 | |
| -15 V | 0 | 1 | 0 | 0 | |
| -30 V | 0 | 1 | 0 | 1 | |
| -12 V | 0 | 1 | 1 | 0 | |
| A3 AGC | 0 | 1 | 1 | 1 | |
| REF OOL | 1 | 0 | 0 | 0 | Selected by LK3 |
| BFO OOL | 1 | 0 | 0 | 1 | Selected by LK4 |
| SYNTH OOL | 1 | 0 | 1 | 0 | Selected by LK5 |
| Not Used | 1 | 0 | 1 | 1 | |
| | 1 | 1 | 0 | 0 | |
| | 1 | 1 | 0 | 1 | |
| | 1 | 1 | 1 | 0 | |
| | 1 | 1 | 1 | 1 | |

28. The voltage chosen for measurement is taken from pin 1 of U31 to W6 P1 to be D-A converted on the Main IF/AF board (A4) for measurement by the microprocessor (see Chapter 5, paras. 32 and 33). After D-A conversion, the comparator output is returned to the A9A2 board on W6P1 pin 5, inverted by U21a and buffered by U15 to be read by the microprocessor. When U15 pin 3 goes low, the microprocessor stops the process and the binary number produced just prior to U15 pin 3 going low, represents the voltage being measured.

Preset Mode Procedure

29. Certain receiver operating parameters may be preset for each mode so that the receiver will automatically return to the selected parameters each time a particular mode is selected. To preset the mode parameters, a board-mounted DIL switch S1a located on the front panel memory board must be temporarily set to the CLOSED position. If this switch is permanently left in the CLOSED position, then the preset mode parameter facility is inhibited. The procedure for presetting the mode parameters is as follows.

30. (1) Set switch S1a on the front panel board to the CLOSED position.

(2) Press the required mode pushbutton (ISB/LSB, ISB/USB, LSB, AM, CW or FM).

(3) Select the required AGC pushbutton(s) i.e. LONG, MEDIUM, SHORT and/or MAN. Note that different AGC time constants may be selected for the two ISB sidebands.

(4) For the AM, CW, FM and AUX modes, select the required IF bandwidth (BW1 to BW5 pushbuttons). Note that the SSB bandpass tuning facility, which uses BW1 or BW2, cannot be preset.

(5) For the CW mode press the BFO pushbutton and rotate the tuning control for the required BFO offset frequency. Press the BFO pushbutton again to disengage the tuning control.

(6) Return switch S1a on the front panel memory board to the OPEN position.

(7) The preset parameters will now be recalled each time a mode is selected, but may be changed by the operator at any time as for normal receiver operation.

A9A2 Link Settings

31. Linking arrangements on the A9A2 board for the 'old' and 'new' A7 and A8 boards are shown on Table 10.

## TABLE 10 A9A2 LINK SETTINGS

| | | |
|---|---|---|
| OLD A8 BOARD | LK1 | B - C |
| | LK2 | B - A |
| | LK3 | B - A |
| | LK4 | B - A |
| NEW A8 BOARD | LK1 | B - A |
| | LK2 | B - C |
| | LK3 | B - C |
| | LK4 | B - C |
| OLD A7 Synthesizer board (Mk 3) | LK5 | B - C |
| | LK6 | B - A |
| NEW A7 (LS1) Synthesizer board (Mk 4) | LK5 | B - A |
| | LK6 | broken |

## FRONT PANEL MEMORY BOARD (ST 82920)

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R1 | 4 k7 | Metal Oxide | ¼ | 2 | 913490 |
| R2 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R3 | 270 | Metal Oxide | ¼ | 2 | 910391 |
| R4 | 47 k | Metal Oxide | ¼ | 2 | 913496 |
| R5 | 47 k | Metal Oxide | ¼ | 2 | 913496 |
| R6 | 68 k | Metal Oxide | ¼ | 2 | 916478 |
| R7 | 68 k | Metal Oxide | ¼ | 2 | 916478 |
| R8 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R9 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R10 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R11 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R12 | 1 M | Composition | ¼ | 5 | 929119 |
| R13 | 1 M | Composition | ¼ | 5 | 929119 |
| R14 | 33 k | Metal Oxide | ¼ | 2 | 913495 |
| R15 | 33 k | Metal Oxide | ¼ | 2 | 913495 |
| R16 | 100 k | Metal Oxide | ¼ | 2 | 915190 |
| R17 | 12 k | Metal Oxide | ¼ | 2 | 917952 |
| R18 | 12 k | Metal Oxide | ¼ | 2 | 917952 |
| R19 | 100 k | Metal Oxide | ¼ | 2 | 915190 |
| R20 | 2k2 | Metal Oxide | ¼ | 2 | 916456 |
| R21 | 2k2 | Metal Oxide | ¼ | 2 | 916456 |
| R22 | 180 | Metal Oxide | ¼ | 2 | 915465 |
| R23 | 180 | Metal Oxide | ¼ | 2 | 915465 |
| R24 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R25 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R26 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R27 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R28 | 4 k7 | Metal Oxide | ¼ | 2 | 913490 |
| R29 | 4 k7 | Metal Oxide | ¼ | 2 | 913490 |
| R30 | 4 k7 | Metal Oxide | ¼ | 2 | 913490 |
| R31 | 4 k7 | Metal Oxide | ¼ | 2 | 913490 |
| R32 | 4 k7 | Metal Oxide | ¼ | 2 | 913490 |
| R33 | 4k7 | Metal Oxide | ¼ | 2 | 913490 |
| R34 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R35 | 27 k | Metal Oxide | ¼ | 2 | 913494 |
| R36 | 27 k | Metal Oxide | ¼ | 2 | 913494 |
| R37 | 18 k | Metal Oxide | ¼ | 2 | 900994 |
| R38 | 68 k | Metal Oxide | ¼ | 2 | 916478 |
| R39 | 68 k | Metal Oxide | ¼ | 2 | 916478 |
| R40 | 22 k | Metal Oxide | ¼ | 2 | 913493 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R41 | 47 k | Metal Oxide | ¼ | 2 | 913486 |
| R42 | 47 k | Metal Oxide | ¼ | 2 | 913496 |
| R43 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R44 | 12 k | Metal Oxide | ¼ | 2 | 917952 |
| R45 | 33 k | Metal Oxide | ¼ | 2 | 913495 |
| R46 | 12 k | Metal Oxide | ¼ | 2 | 917952 |
| R47 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R48 | 18 k | Metal Oxide | ¼ | 2 | 900994 |
| R49 | 4 k7 | Metal Oxide | ¼ | 2 | 913490 |
| R50 | 20k | RESVAR | ¼ | 5 | 943434 |
| R51 | 20k | RESVAR | ¼ | 5 | 943434 |
| **Capacitors** | | | Volts | | |
| C1 | 0µ1 | Disc Ceramic | 50 | 20 | 938406 |
| C2 | 0µ1 | Disc Ceramic | 50 | 20 | 938406 |
| C3 | 0µ1 | Disc Ceramic | 50 | 20 | 938406 |
| C4 | | Not used | | | |
| C5 | 0µ1 | Disc Ceramic | 50 | 20 | 938406 |
| C6 | 330 | Electrolytic | 10 | +50 -10 | 939691 |
| C7 | 100 | Electrolytic | 40 | +50 -10 | 940766 |
| C8 | 100 | Electrolytic | 40 | +50 -10 | 940766 |
| C9 | 0µ1 | Disc Ceramic | 50 | 20 | 938406 |
| C10 | 15 p | Ceramic | 500 | 5 | 938522 |
| C11 | 15 p | Ceramic | 500 | 5 | 938522 |
| C12 | 15 | Tantalum | 20 | 20 | 938034 |
| C13 | 1µ0 | Tantalum | 35 | 20 | 938405 |
| C14 | 100 p | Ceramic | 500 | 10 | 938556 |
| C15 | 100 p | Ceramic | 500 | 10 | 938556 |
| **Switches** | | | | | |
| S1 | | 3-pole, DIL | | | 938557 |

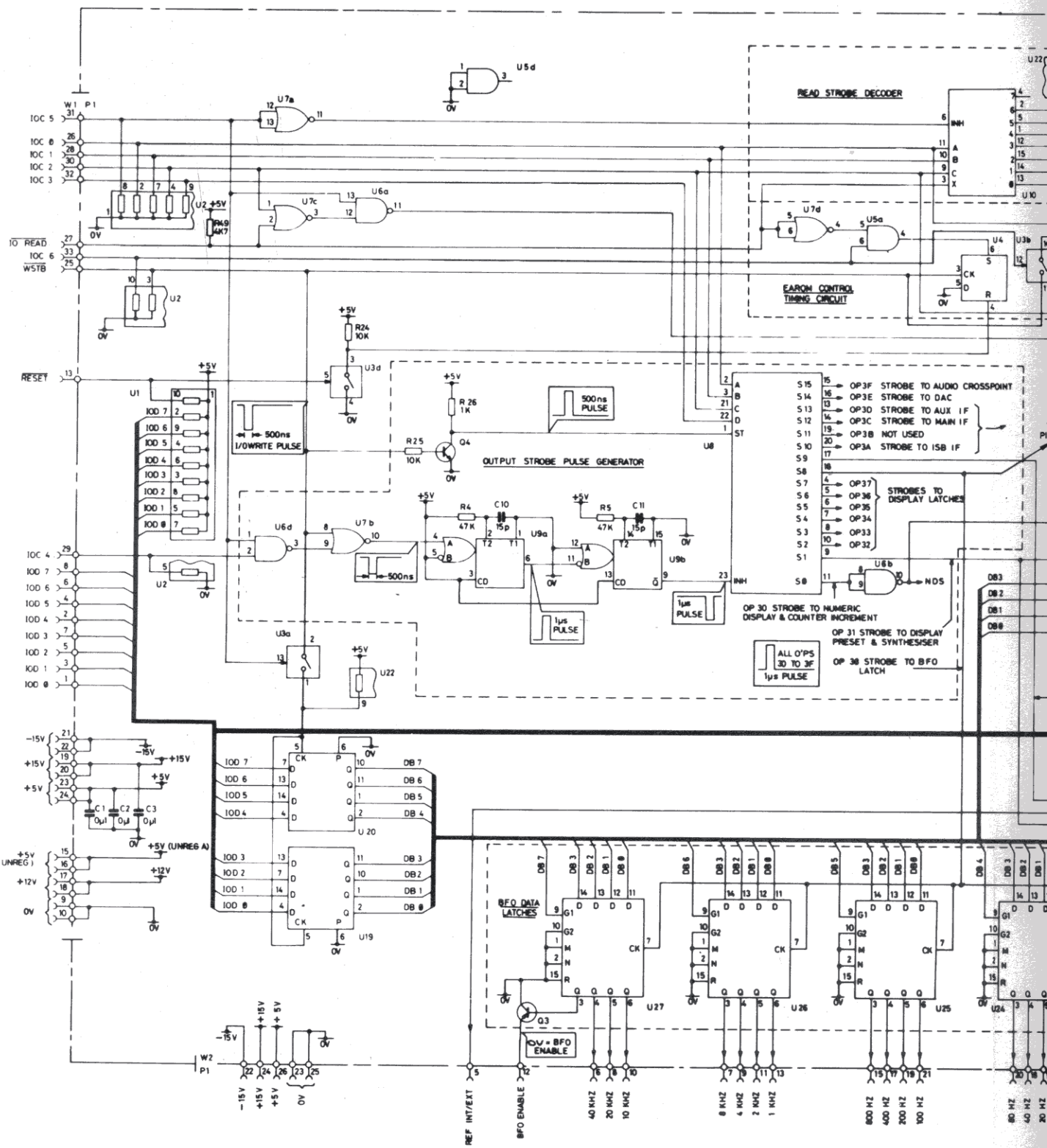
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Connectors** | | | | | |
| J1 | | Plug, 26-way | | | 938569 |
| J2 | | Plug, 50-way | | | 938570 |
| W1 | | Cable assembly | | | B08227 |
| | | Comprising: | | | |
| | | Connector, Plug PCB 34-way | | | 938571 |
| | | Socket, 34-way | | | 934213 |
| | | Clamp, Strain relief | | | 934214 |
| | | Cable flat, 34-way | | | 927065 |
| W2 | | Cable assembly | | | B08368 |
| | | Comprising: | | | |
| | | Connector, Plug PCB 26-way | | | 938572 |
| | | Socket, 26-way | | | 935019 |
| | | Clamp, Strain relief | | | 935020 |
| | | Cable, flat, 26-way | | | 927429 |
| W5 | | Cable assembly | | | B08714 |
| | | Comprising: | | | |
| | | Connector, Plug PCB 20-way | | | 938062 |
| | | Socket, 20-way | | | 935017 |
| | | Clamp, Strain relief | | | 935018 |
| | | Cable, flat, 20-way | | | 927303 |
| W6 | | Cable assembly | | | B08363 |
| | | Comprising: | | | |
| | | Connector, Plug PCB 40-way | | | 938574 |
| | | Socket, 40-way | | | 935021 |
| | | Clamp, Strain relief | | | 935022 |
| | | Cable, flat, 40-way | | | 927302 |
| **Transistors** | | | | | |
| Q1 | | PNP Silicon 2N2906A | | | 920963 |
| Q2 | | PNP Silicon 2N2906A | | | 920963 |
| Q3 | | 2N3906 | | | 914047 |
| Q4 | | NPN Silicon 2N2369 | | | 906842 |

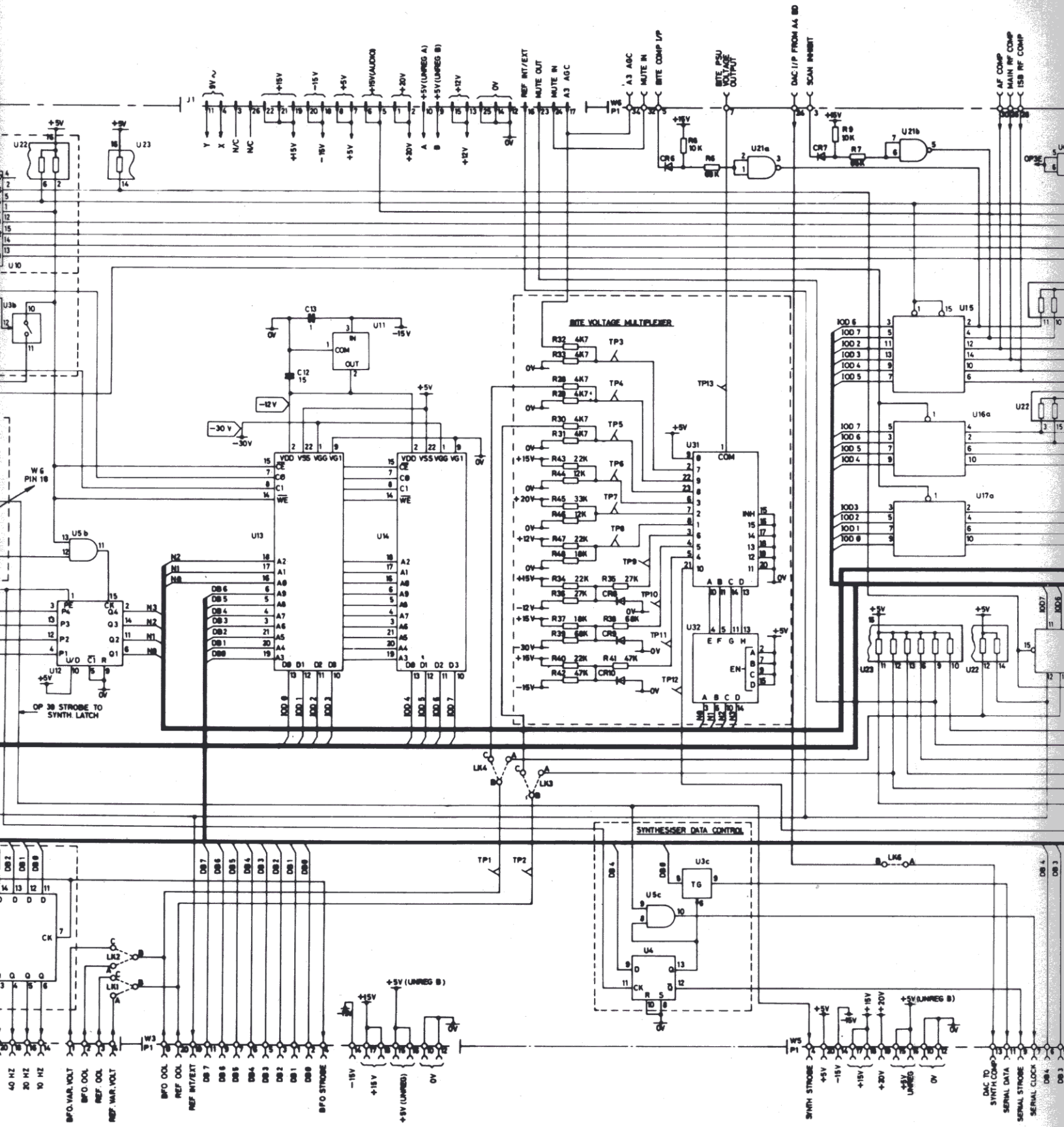
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Diodes** | | | | | |
| CR1 | | Silicon 1N916 | | | 913480 |
| CR2 | | Silicon 1N4001 | | | 915266 |
| CR3 | | Silicon 1N916 | | | 913480 |
| CR4 | | Silicon 1N916 | | | 913480 |
| CR5 | | Zener, 30 V, 5% | | | 937983 |
| CR6 | | Silicon 1N916 | | | 913480 |
| CR7 | | Silicon 1N916 | | | 913480 |
| CR8 | | Silicon 1N4149 | | | 923222 |
| CR9 | | Silicon 1N4149 | | | 923222 |
| CR10 | | Silicon 1N4149 | | | 923222 |
| **Integrated Circuits** | | | | | |
| U1 | | 10 k SIL Resistor network | | | 938558 |
| U2 | | 10 k SIL Resistor network | | | 938558 |
| U3 | | Quad transmission gate 4066 | | | 930148 |
| U4 | | Dual D-type flip-flop 4013 | | | 933644 |
| U5 | | Quad 2-input AND gate 4081 | | | 938559 |
| U6 | | Quad 2-input NAND gate 4011 | | | 938560 |
| U7 | | Quad 2-input NOR gate 4001 | | | 930027 |
| U8 | | 4 to 16 Decoder/Demultiplexer 4514 | | | 931010 |
| U9 | | Dual Monostable 14528 | | | 938562 |
| U10 | | Single 8-channel multiplexer 4051 | | | 929383 |
| U11 | | -12 V regulator 79M12 | | | 938563 |
| U12 | | Binary up/down counter 4516 | | | 938564 |
| U13 | | 1 k x 4-bit EAROM ER3400 | | | 934622 |
| U14 | | 1 k x 4-bit EAROM ER3400 | | | 934622 |
| U15 | | Hex tri-state buffer 14503 | | | 931004 |
| U16 | | Hex tri-state buffer 14503 | | | 931004 |
| U17 | | Hex tri-state buffer 14503 | | | 931004 |
| U18 | | Hex tri-state buffer 14503 | | | 931004 |
| U19 | | Quad D-type Latch 4042 | | | 930861 |
| U20 | | Quad D-type Latch 4042 | | | 930861 |
| U21 | | Dual 2-input NAND buffer 40107 | | | 931052 |
| U22 | | 10 k DIL resistor network | | | 938565 |
| U23 | | 10 k DIL resistor network | | | 938565 |
| U24 | | 4-bit tri-state 'D' type register | | | 931000 |
| U25 | | 4-bit tri-state 'D' type register | | | 931000 |

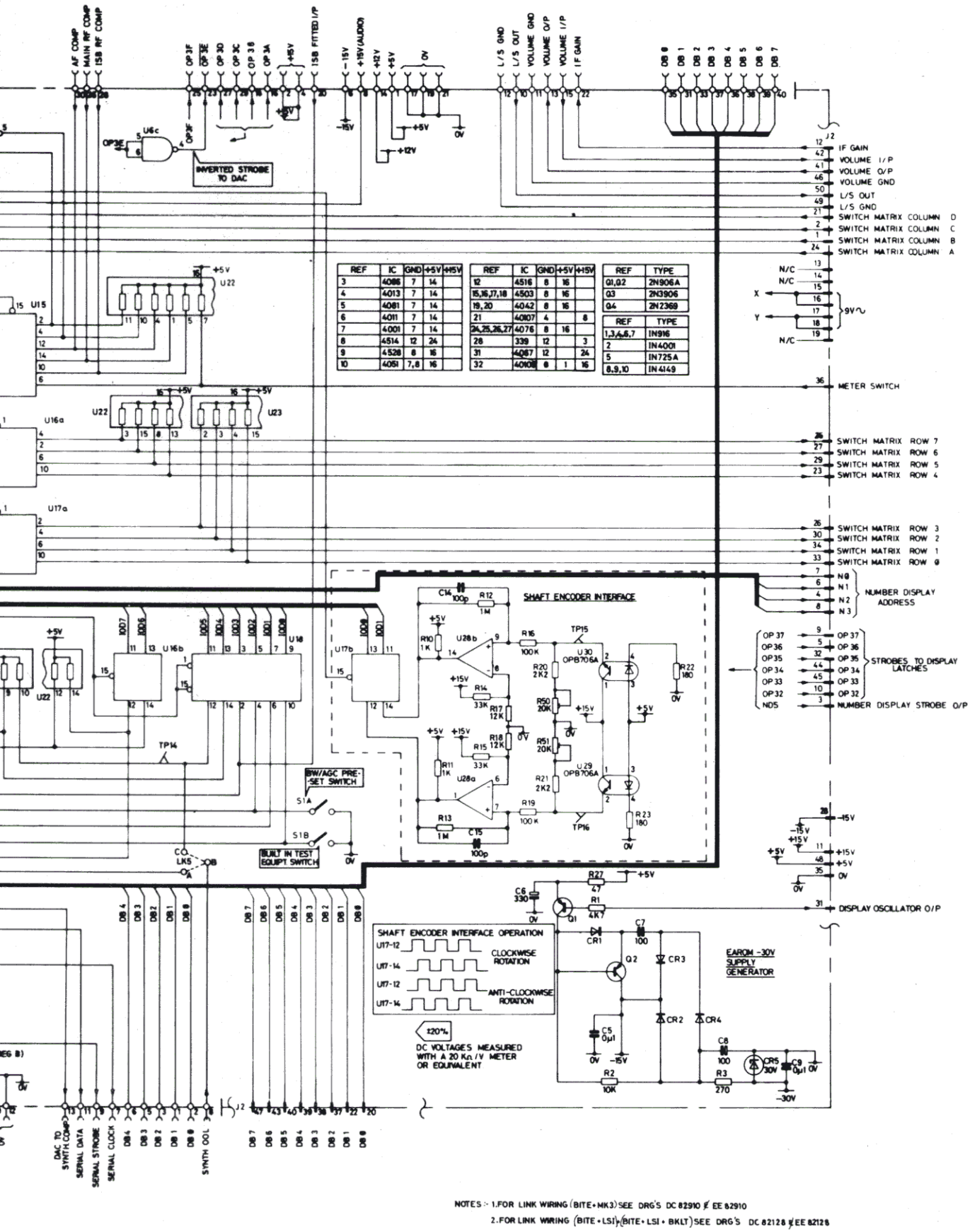
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| U26 | | 4-bit tri-state 'D' type register | | | 931000 |
| U27 | | 4-bit tri-state 'D' type register | | | 931000 |
| U28 | | Quad comparator LM339J | | | 929149 |
| U29 | | Optical switch OPB706A | | | 938567 |
| U30 | | Optical switch OPB706A | | | 938567 |
| U31 | | 16 channel analog 4067 | | | 930998 |
| U32 | | Quad low to high level | | | 931054 |

Miscellaneous

| | | | | | |
|---|---|---|---|---|---|
| | | 8-pin DIL IC socket | | | 940901 |
| | | 14-pin DIL IC socket | | | 940902 |
| | | 16-pin DIL IC socket | | | 940903 |
| | | 22-pin DIL IC socket | | | 930608 |
| | | 24-pin DIL IC socket | | | 930609 |


READ STROBE DECODER
EAROM CONTROL TIMING CIRCUIT
OUTPUT STROBE PULSE GENERATOR
OP 30 STROBE TO NUMERIC DISPLAY & COUNTER INCREMENT
OP 31 STROBE TO DISPLAY PRESET & SYNTHESISER
OP 38 STROBE TO BFO LATCH
STROBES TO DISPLAY LATCHES
BFO DATA LATCHES
BFO ENABLE
REF INT/EXT
IOC 5
IOC 6
IOC 1
IOC 2
IOC 3
IO READ
WSTB
RESET
500ns I/OWRITE PULSE
500ns PULSE
1µs PULSE
ALL O'PS 30 TO 3F 1µs PULSE
OP3F STROBE TO AUDIO CROSSPOINT
OP3E STROBE TO DAC
OP3D STROBE TO AUX IF
OP3C STROBE TO MAIN IF
OP3B NOT USED
OP3A STROBE TO ISB IF
OP37
OP36
OP35
OP34
OP33
OP32
NDS
+5V (UNREG A)
40 KHZ
20 KHZ
10 KHZ
8 KHZ
4 KHZ
2 KHZ
1 KHZ
800 HZ
400 HZ
200 HZ
100 HZ
80 HZ
40 HZ
20 HZ


BITE VOLTAGE MULTIPLEXER
SYNTHESISER DATA CONTROL
OP 38 STROBE TO SYNTH. LATCH
W6 PIN 18
REF INT/EXT
MUTE OUT
MUTE IN
A3 AGC
BITE COMP I/P
BITE PSU VOLTAGE OUTPUT
DAC I/P FROM A4 BD
SCAN INHIBIT
AF COMP
MAIN RF COMP
ISB RF COMP
BFO VAR. VOLT
BFO OOL
REF OOL
REF. VAR. VOLT
BFO STROBE
SYNTH STROBE
DAC TO SYNTH COMP
SERIAL DATA
SERIAL STROBE
SERIAL CLOCK
+5V (UNREG B)




| REF | IC | GND | +5V | +15V |
|---|---|---|---|---|
| 3 | 4086 | 7 | 14 | |
| 4 | 4013 | 7 | 14 | |
| 5 | 4081 | 7 | 14 | |
| 6 | 4011 | 7 | 14 | |
| 7 | 4001 | 7 | 14 | |
| 8 | 4514 | 12 | 24 | |
| 9 | 4528 | 8 | 16 | |
| 10 | 4051 | 7,8 | 16 | |

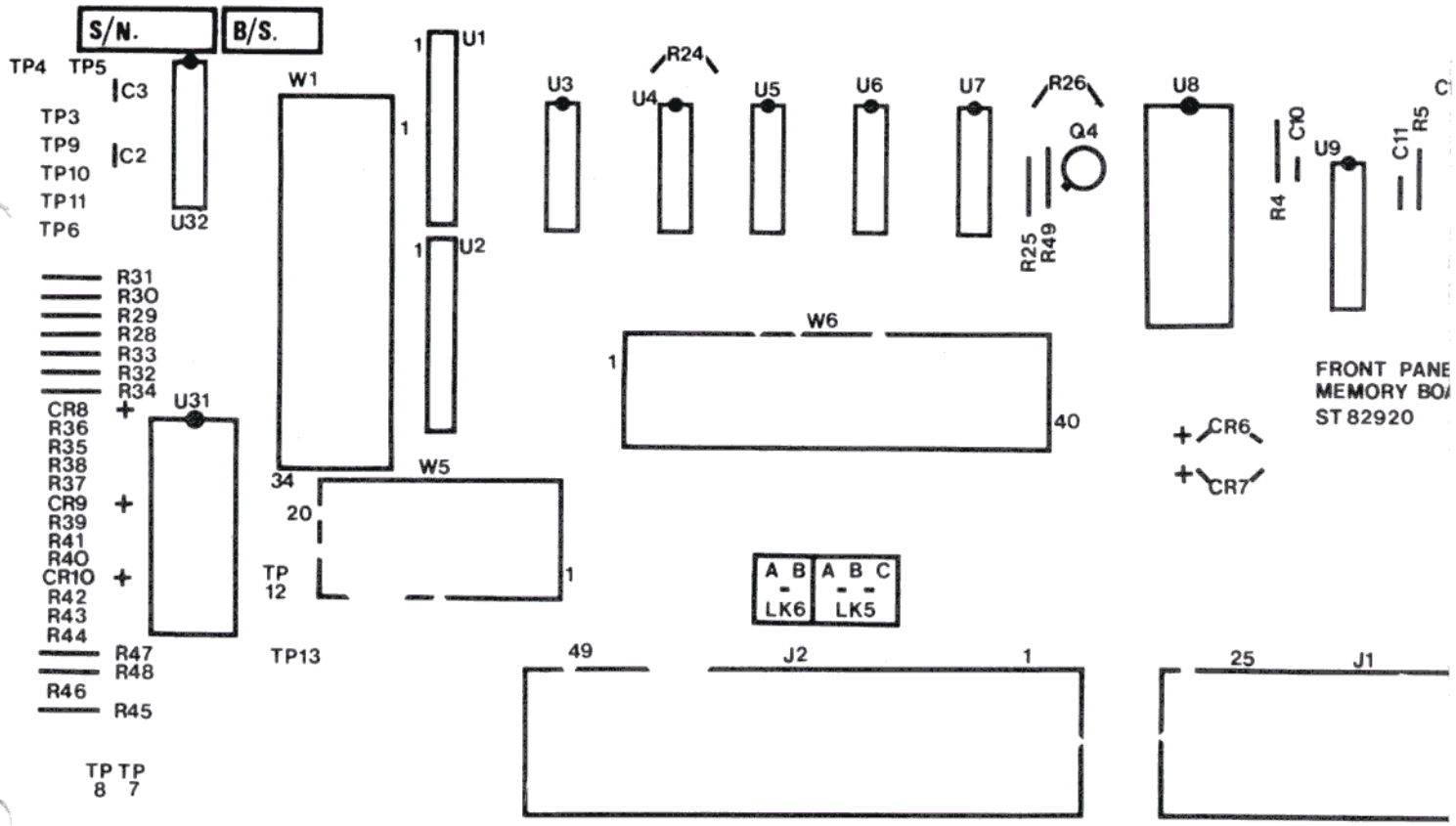
| REF | IC | GND | +5V | +15V |
|---|---|---|---|---|
| 12 | 4516 | 8 | 16 | |
| 15,16,17,18 | 4503 | 8 | 16 | |
| 19,20 | 4042 | 8 | 16 | |
| 21 | 40107 | 4 | | 8 |
| 24,25,26,27 | 4076 | 8 | 16 | |
| 28 | 339 | 12 | | 3 |
| 31 | 4067 | 12 | | 24 |
| 32 | 40108 | 8 | 1 | 16 |

| REF | TYPE |
|---|---|
| Q1,Q2 | 2N3906A |
| Q3 | 2N3906 |
| Q4 | 2N2369 |

| REF | TYPE |
|---|---|
| 1,3,4,6,7 | IN916 |
| 2 | IN4001 |
| 5 | IN725A |
| 8,9,10 | IN4149 |

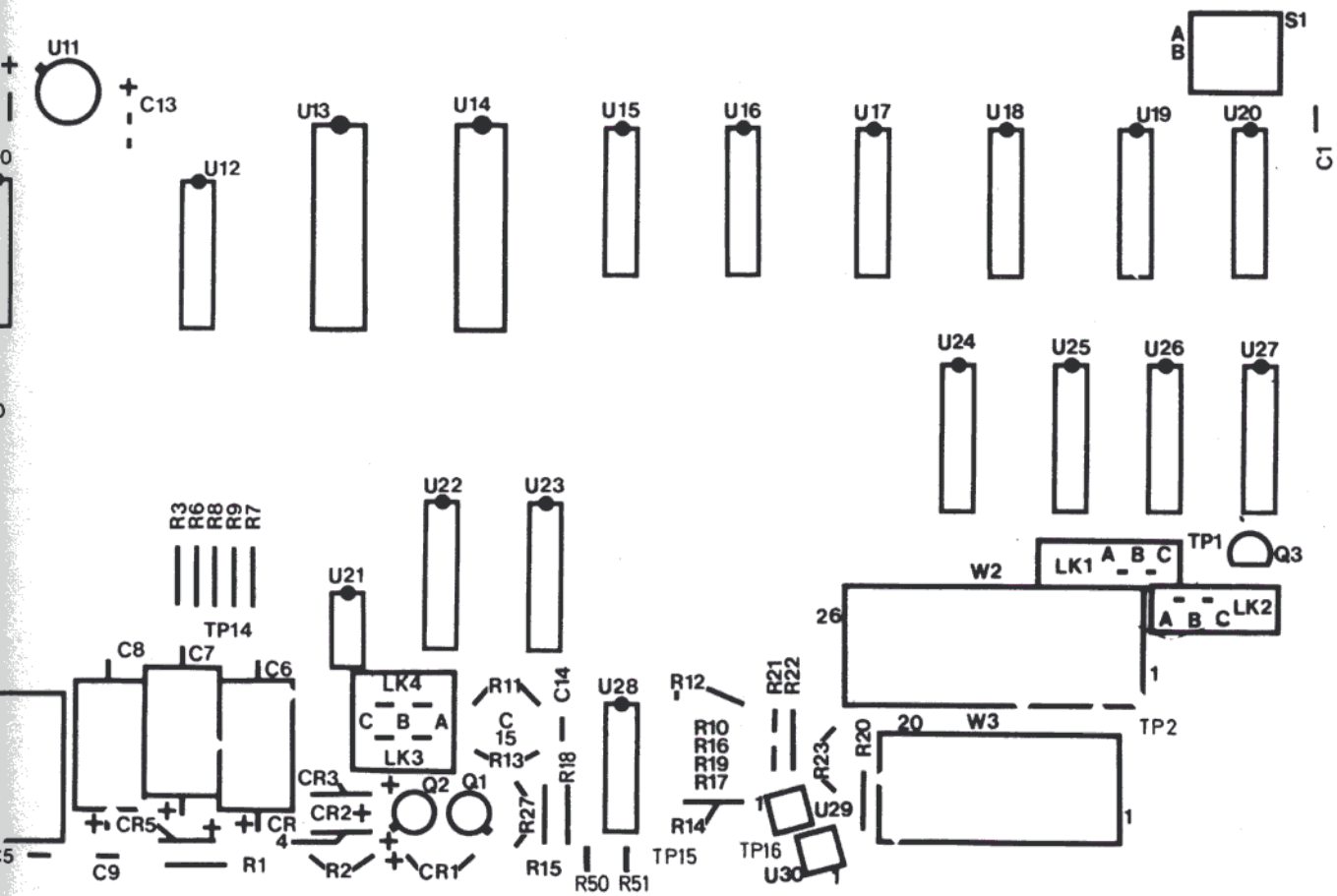
NOTES :- 1.FOR LINK WIRING (BITE+MK3) SEE DRG'S DC 82910 & EE 82910
2.FOR LINK WIRING (BITE+LSI)-(BITE+LSI+BKLT) SEE DRG'S DC 82128 & EE 82128

# Circuit : Front Panel Memory Board
# A9A2 Fig. 10.1




RACAL

| TH 3416 | EA82919 |
|---|---|
| 3 | 8 |




Component Layout:
Front Panel Memory Board Fig.10.2

# CHAPTER 11

# AC POWER SUPPLY UNIT A10

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| 3 | CIRCUIT DESCRIPTION | 11-1 |
| 6 | REPLACEMENT OF LAMPS | 11-1 |
| | Components List | |


## ILLUSTRATIONS


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|---|---|
| 11-1 | Circuit: AC Power Supply Unit A10 |
| 11-2 | Component Layout: AC Power Supply Unit A10 |

# CHAPTER 11

# AC POWER SUPPLY UNIT A10

## INTRODUCTION

1. The self contained power supply unit A10 provides regulated outputs at +20 V, +15 V, +12 V, +5 V and -15 V Fused, unregulated outputs of +15 V and +5 V are also available. A line filter is provided for the reduction of mains-borne interference and the unit will operate from inputs of 100 V, 120 V, 220 V or 240 V nominal.

2. As supplied the receiver is fitted with resistors R3 and R4 3.3 ohms. This produces the maximum permissible display brightness. The brightness may be reduced by increasing the value of R3 and R4. These resistors are fitted on the outside of the power supply (see Fig. 11.2). Before attempting to change these resistors, remove the mains supply connector.

## CIRCUIT DESCRIPTION

3. AC power is applied to the unit through J1, FS1 and the line filter. The voltage selector allows connection of 100 V, 120 V, 220 V or 240 V by means of a printed-circuit card which fits one of 4 ways into a holder, thereby arranging a suitable transformer primary connection (T1). One of the three secondary windings on T1 supplies a pre-regulator consisting of Q1 and associated components, after which the DC is applied to U5, a +20 V monolithic voltage regulator. A second secondary winding on T1 supplies the +5 V regulator and the third winding supplies the +15 V, +12 V and -15 V regulators.

4. The three-terminal monolithic voltage regulators used in this module, each contain a current-limiting circuit to maintain the peak current passed to within a safe value. If the internal dissipation becomes too high for the heat sinking provided, a thermal shutdown circuit takes over to prevent damage to the regulator. The shutdown circuit resets automatically, operating again if conditions remain unfavourable.

5. A 6.8 V zener diode, CR4, is included to provide over-voltage protection for the +5 V supply. This diode is a stud-mounted type. The two 1 A fuses A10 A1 FS2 and A10 A1 FS3, for the +5 V and +15 V unregulated supplies respectively, are wire link fuses mounted on the connector board, together with the output connector A10A1J1 which connects with the front panel memory board. The power input connector A10J1 in mounted on the rear panel together with the voltage selector and fuse A10FS1. The output connector A1J1 connects with the front panel memory board.

## REPLACEMENT OF LAMPS

6. (1) Remove power connectors.

   (2) Remove push on caps from control knobs.

   (3) Remove screw behind large tuning knob and further four screws securing front panel.

   (4) Unplug appropriate display exposing the lamp board.

   (5) Remove the two screws and washers securing the board and withdraw the board.

# AC POWER SUPPLY MODULE A10 (ST 82922)

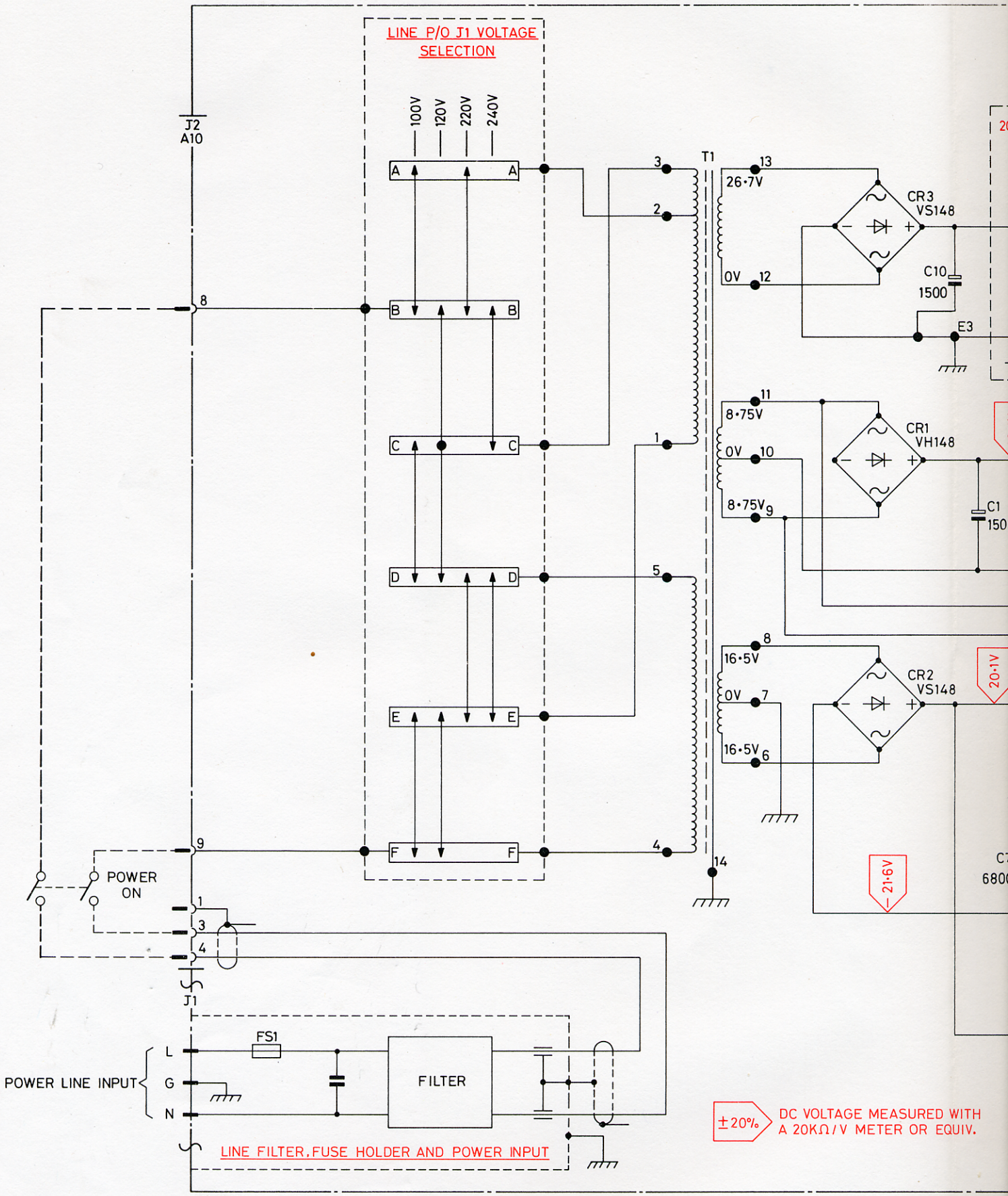
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R1 | 33 | Metal Oxide | ¼ | 2 | 917060 |
| R2 | | Not Used | | | |
| * R3 | 3.3 | Wirewound | 2.5 | | 917143 |
| * R4 | 3.3 | Wirewound | 2.5 | | 917143 |
| **Capacitors** | | | V | | |
| C1 | 15,000 | Electrolytic | 25 | | 943155 |
| C2 | 1 | Tantalum | 35 | 20 | 943726 |
| C3 | 1 | Tantalum | 35 | 20 | 943726 |
| C4 | 6800 | Electrolytic | 40 | | 943154 |
| C5 | 1 | Tantalum | 35 | 20 | 943726 |
| C6 | 1 | Tantalum | 35 | 20 | 943726 |
| C7 | 6800 | Electrolytic | 40 | | 943154 |
| C8 | 1 | Tantalum | 35 | 20 | 943726 |
| C9 | 6.8 | Tantalum | 35 | 20 | 943727 |
| C10 | 1500 | Electrolytic | 63 | | 943153 |
| C11 | 1 | Tantalum | 35 | 20 | 943726 |
| C12 | 1 | Tantalum | 35 | 20 | 943726 |
| C17 | 0.01 | Ceramic Disc | 250 | | 900067 |
| **Diodes** | | | | | |
| CR1 | | VH148 | | | 938491 |
| CR2 | | VS148 | | | 938492 |
| CR3 | | VS148 | | | 938492 |
| CR4 | | Z3B 6.8 R | | | 940045 |
| **Integrated Circuits** | | | | | |
| U1 | | µA78H05KC +5 V Regulator | | | 938498 |
| U2 | | µA7815KC +15 V Regulator | | | 932797 |
| U3 | | µA7915KC -15 V Regulator | | | 938024 |
| U4 | | 7812K2 +12 V Regulator | | | 923014 |
| **Transformer** | | | | | |
| T1 | | | | | CT81412 |

* Value dependent on brightness required

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Connectors** | | | | | |
| J1 | | Plug, 3-way, filtered inlet | | | 937173 |
| J2 | | Socket, 9-way | | | 918090 |
| **Miscellaneous** | | | | | |
| FS1 | | Fuse 1 A 250 V Slo-blow | | | 938493 |
| XF1 | | Fuseholder | | | 938495 |
| | | 20 V Regulator Board | | | ST82991 |
| | | Comprising: | | | |
| C17 | | Capacitor Ceramic | 250 | +40 -20 | 916187 |
| J3 | | Socket, 25-way | | | 930819 |
| FS2 | | Wire BTC 40 SWG | | | 909807 |
| FS3 | | Wire BTC 40 SWG | | | 909807 |
| | | A10A1 Connector Assembly | | | B08160 |
| | | Comprising: | | | |
| | | Socket, 25-way | | | 930819 |
| | | Connection Board | | | BA80777 |
| | | Mating socket for J1 (POWER IN) | | | 930766 |

## 20 VOLT REGULATOR BOARD ST 82993

| | ohms | | W | | |
|---|---|---|---|---|---|
| **Resistors** | | | | | |
| R2 | 4k7 | Metal Oxide | ¼ | 2 | 913490 |
| | **µF** | | **V** | | |
| **Capacitors** | | | | | |
| C13 | 0.01 | Ceramic | 50 | | 938053 |
| C14 | 6.8 | Tantalum | 50 | | 943427 |
| C15 | 1 | Tantalum | 50 | | 926785 |
| C16 | 6.8 | Tantalum | 50 | | 943427 |
| **Diodes** | | | | | |
| CR5 | | Zener, BZX79-C27 | | | 930321 |
| **Integrated Circuit** | | | | | |
| U5 | | 78M20 (+20 volt reg) | | | 938642 |
| **Transistor** | | | | | |
| Q1 | | MJE 800 | | | 938641 |

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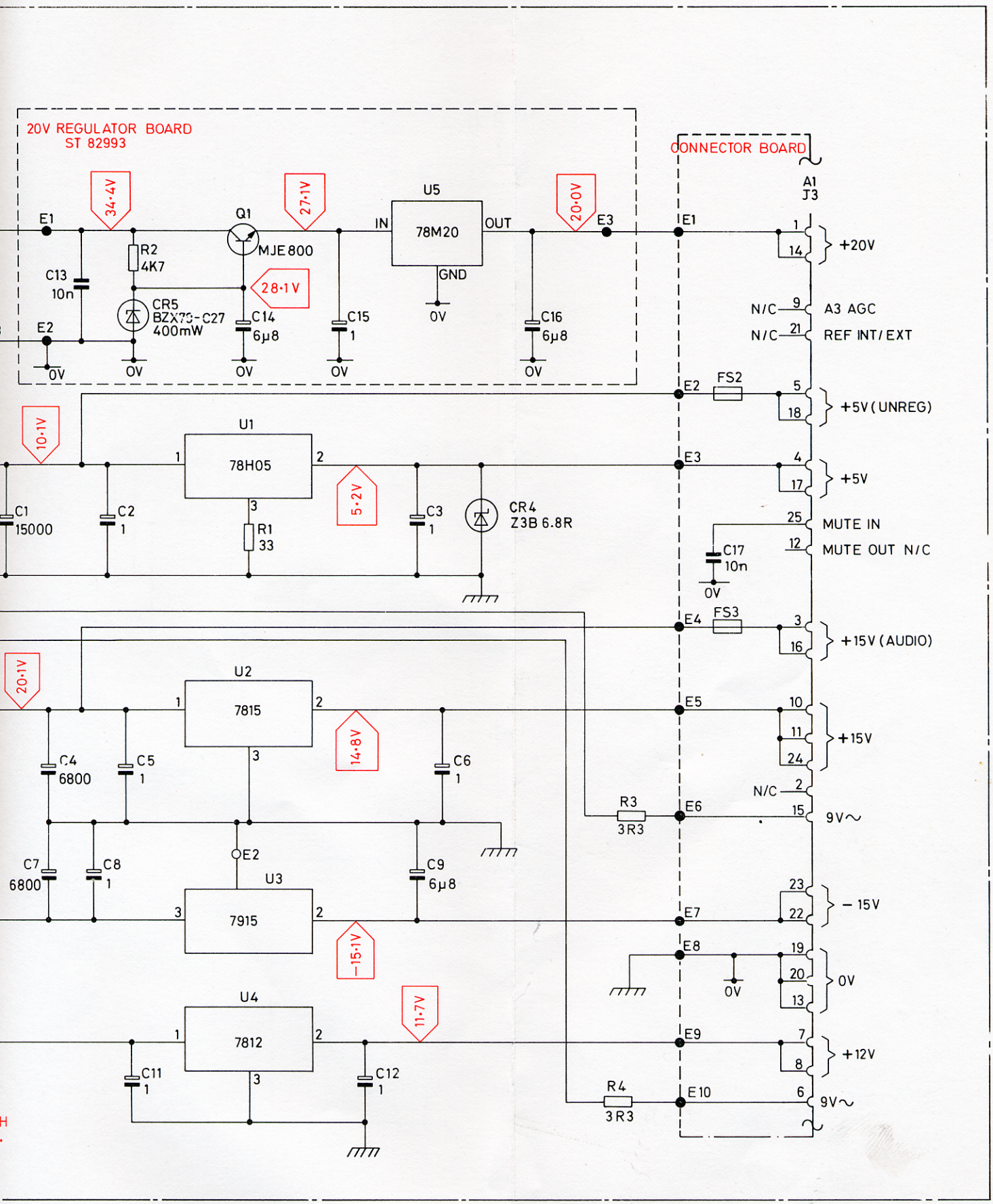
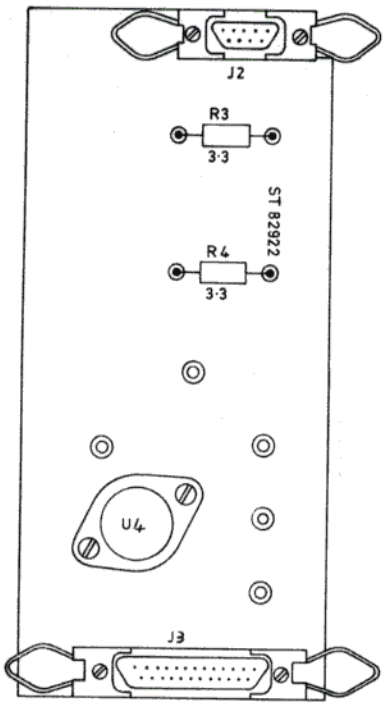
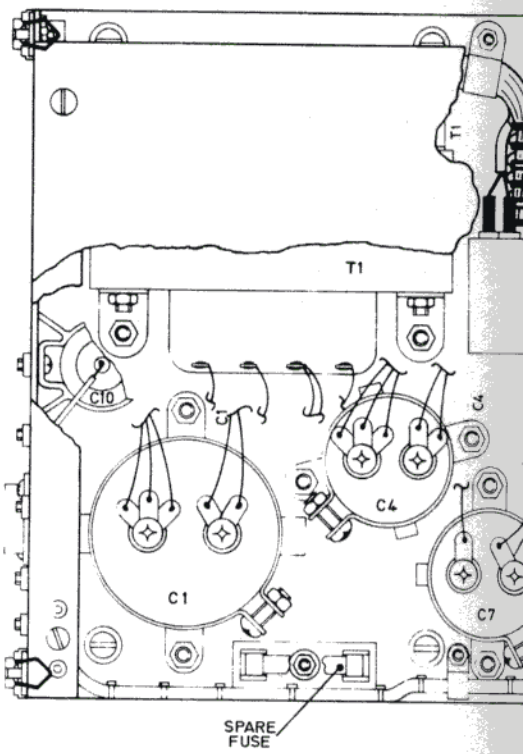
| TH 3416 | DC 82922 |
|---|---|
| 2 \| 4 | |

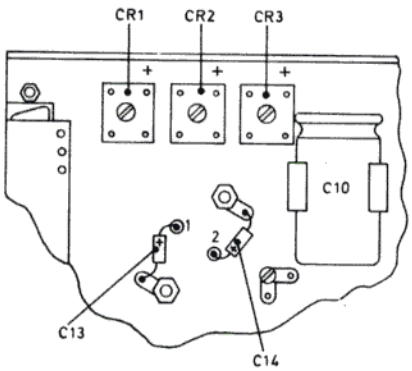
| TH 3416 | DC08719/2 |
|---|---|
| 6 \| 4 | |



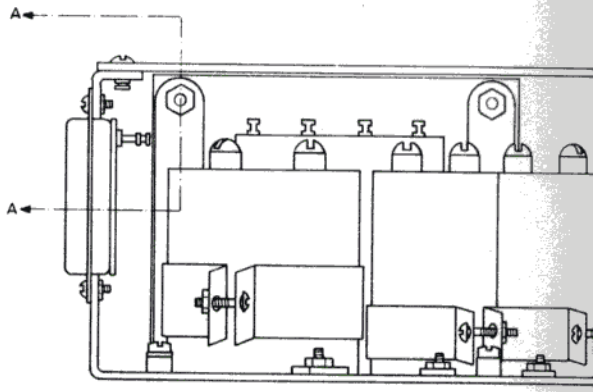

Circuit: AC Power Supply Fig.11.1

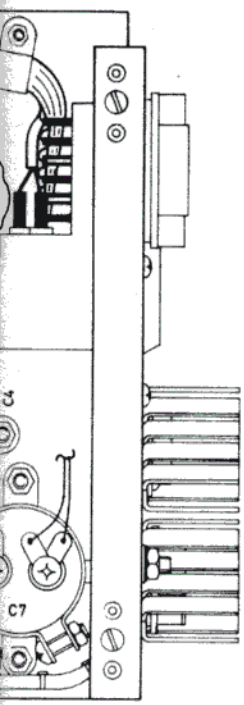

J2
R3
3·3
ST 82922
R4
3·3
U4
J3

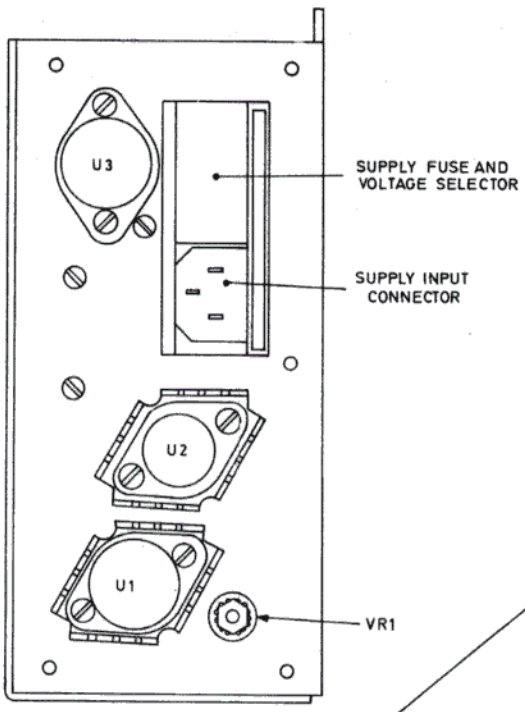

T1
C10
C4
C1
C7
SPARE
FUSE

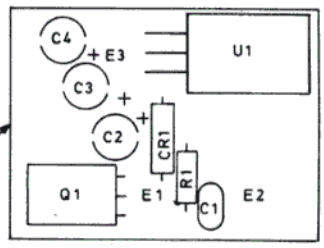

CR1
CR2
CR3
C10
1
2
C13
C14

SECTION A-A

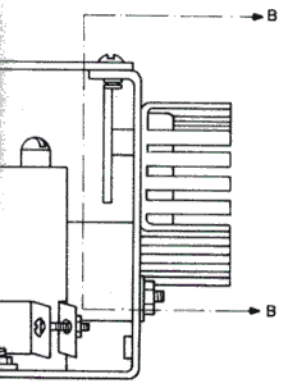

A
A

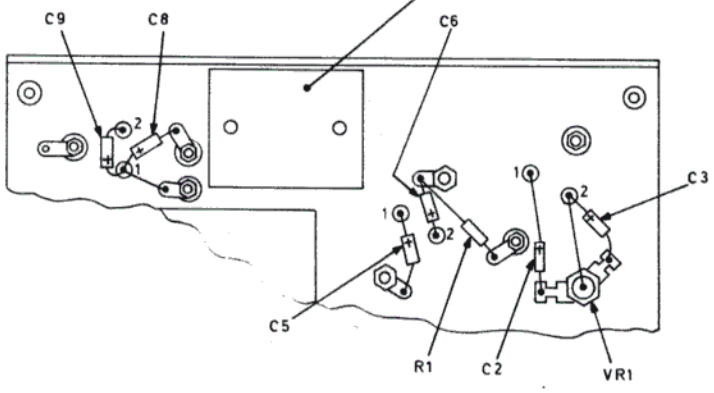



20V REGULATOR BOARD
( A10A2 - B08717 )




SECTION B-B

**Component Layout:**
**AC Power Supply Module A10** **Fig.11.2**

# CHAPTER 12

# FREQUENCY STANDARD A11

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## ILLUSTRATIONS


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|---|---|
| 12-1 | Circuit & Layout: Frequency Standard Module A11 |

# CHAPTER 12

# FREQUENCY STANDARD A11

## INTRODUCTION

1. The 5 MHz Frequency Standard provides high accuracy and long term stability with low power consumption. The crystal is mounted in a proportional temperature controlled oven which together with stabilised, low excitation maintaining circuit and buffer amplifier, is fitted in a 2 x 2 x 2 inch can with polyurethane foam to provide heat insulation. The standard operates from the +12 V supply.

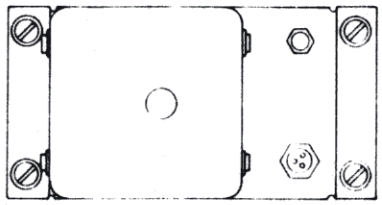
## APPLICATION

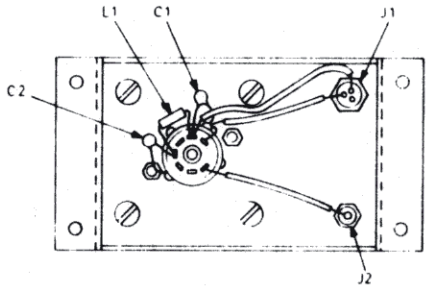
2. The A11 module is fitted as standard to the RA 1792 Receiver, and provides reference for the second LO/BFO Synthesizer board (module A8). An alternative reference may be provided from a TXCO unit fitted directly on the A8 board, or an external reference of 1 MHz, or 5 MHz or 10 MHz may be connected to J1 of the A8 module.

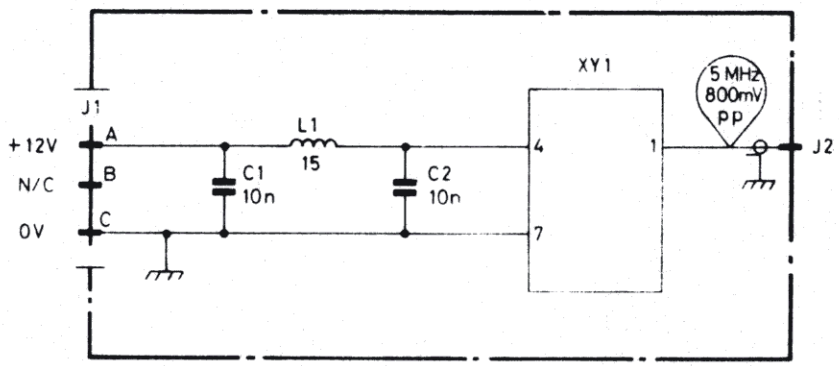
## FREQUENCY STANDARD MODULE A11 (ST 08140)

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Capacitors** | | | | | |
| C1 | 0.01 | Ceramic | | 20 | 938035 |
| C2 | 0.01 | Ceramic | | 20 | 938035 |
| **Inductors** | | | | | |
| L1 | 15 µH | Choke Fixed RF | | | 915850 |
| **Frequency Standard** | | | | | |
| *Y1 | | 9442/12 | | | 933706 |
| **Connectors** | | | | | |
| J1 | | Plug, 3-way | | | 938471 |
| J2 | | Plug, Coaxial RF | | | 938472 |
| XY1 | | Socket 7-way | | | 938473 |

* This item is not supplied with Frequency Module ST 08140 as the type varies with the particular option fitted.






RACAL
TM1496 BC08141
1 3

Circuit & Layout:
Frequency Standard Module A11

Fig. 12.1

# CHAPTER 13

# ALIGNMENT PROCEDURES

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|---|---|
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# CHAPTER 13

# ALIGNMENT PROCEDURES

## INTRODUCTION

1. This chapter contains alignment procedures for the RA 1792 Receiver as a complete assembly. Under normal operating conditions the receiver will maintain the factory alignment over a long period of time. Realignment should, therefore, only be carried out following the replacement of components which affect the alignment, or where a known misalignment exists. Refer to RA 1792/MA 1075 Operators Handbook for operating instructions.

2. Should it be necessary to realign the complete receiver, the following procedures must be followed in the order given. Before attempting to realign an individual sub-assembly it must be ascertained, where applicable, that the preceding assemblies are functioning correctly.

3. If the specified performance cannot be attained by alignment, then a fault must be suspected and reference should be made to Chapter 14, Fault Location.

4. A certain amount of dismantling is necessary to gain access to certain areas of the receiver. Details for dismantling and reassembly are contained in paragraph 6. After alignment, ensure that all dismantled assemblies are correctly reassembled and that all shielding covers are replaced using all screws provided or their exact equivalents.

5. Table 13-1 lists the test equipment required. Those listed in the example column are recommendations only. Any instruments with equal or better characteristics may be substituted.

## RECEIVER DISASSEMBLY AND REASSEMBLY

6. Figures 13.1 and 13.2 show the location of the printed circuit boards, and the printed circuit layouts will be found at the end of each chapter. To disassemble the receiver proceed as follows:

   (1) Remove the receiver from rack or cabinet. It is held by 4 screws on the front panel.

   (2) Remove top and bottom cover plates by loosening six quarter-turn fasteners.

   (3) The A1, A6A1 and A6A2 modules may now be removed from the chassis by unplugging all electrical connections, removing the screws securing each module, then lifting the module away from the chassis.

   (4) The Power Supply module (A10) may be removed by disconnecting electrical connections, loosening the 4 captive screws holding the module to the chassis, and 5 screws securing the module to the rear panel.

(5) To remove A4 module and/or A5 (optional) module, unplug all electrical connections, remove screws securing the module to the chassis and lift the module out.

(6) To remove either A9A1 or A9A2 modules, remove the five electrical connections from A9A2 that came from modules A6A2, A4, A7, A8 and A10, then remove four screws securing the front panel and front chassis and lower the whole assembly away from the main chassis. Remove the tuning disk from the tuning shaft, located behind module A9A2. Module A9A2 may now be removed by removing the screws securing it to module A9A1.

(7) To remove module A9A1 first perform step 6 above, then remove the IF GAIN and VOLUME control knobs and remove the front panel. The A9A1 module may now be removed from the front chassis plate by removing the screws securing it to that plate.

(8) Figure 13-2 shows a bottom view of the chassis which provides access to modules A2, A3, A7 and A8. To remove either of these four modules, remove the shielding cover and from the respective module compartment, remove its electrical connections and then remove the module by removing the screws securing it to the chassis.

CHECKING PROCEDURE, POWER SUPPLY A10

7. Test Equipment Required: Digital Multimeter, item 1 of Table 13-1; and Oscilloscope, item 2.

Procedure

8. (1) Disconnect the cable from A10A1J1 located on the base of the power supply.

(2) Connect the digital voltmeter, item 1, between chassis (0 V) and each of the following pins of the power supply, A10, in turn. Use the oscilloscope, item 2, to measure the ac ripple.

| A10A1J1 Pin No's | Voltage | AC Ripple (p-p) |
|---|---|---|
| 1, 14 | +20, ±1 V | 5 mV |
| 10, 11, 24 | +15, ±0.75 V | 5 mV |
| 3, 16 | +20 V nominal unregulated | |
| 22, 23 | -15 V, ±0.75 V | 5 mV |
| 7, 8 | +12 V, ±0.5 V | 5 mV |
| 4, 17 | +5 V, +0.5, -0.2 V | 5 mV |
| 5, 18 | +10 V nominal unregulated | 5 mV |
| 13, 19, 20 | Ground, 0 Volts | |

(3) Disconnect all test equipment and reconnect the cable to the power supply.

## ALIGNMENT PROCEDURE - 2nd LO/BFO SYNTHESIZER A8

9. Test Equipment Required: Digital Multimeter, item 1 of Table 13-1, RF Voltmeter, item 3, Digital Frequency Meter, item 5, and Oscilloscope, item 2.

Procedure

10. (1) Check on the A8 board to ensure that the links LK1 and LK2 are made as tabulated below for the required REF Frequency IN/OUT mode of operation.

| Operating I/O | LK1 | LK2 |
|---|---|---|
| 1 MHz | Link | Link |
| 5 MHz | Open | Link |
| 10 MHz | Link | Open |

(2) Check that S2 REF INT/EXT switch on the rear panel is set to INT.

(3) Connect the digital frequency meter to J3 and the digital multimeter, set to the 10 Volt range, between TP5 and ground. Connect the frequency meter 1 MHz input to the receiver REF IN/OUT socket J1.

(4) Check Voltmeter for a reading between 6 to 11 Volts. Check frequency meter for a reading of 40.000000 MHz ± 1 Hz.

(5) Disconnect the frequency meter and measure the 40 MHz output level at J3 into 50 ohms, using the RF Voltmeter. This level should be not less than -5 dBm.

(6) Set the receiver controls for CW operation, and BFO indication to 0.00 kHz.

(7) Connect the digital frequency meter to J4 on the digital multimeter, set to the 10 Volt range, between TP8 and ground.

(8) Observe that the BFO output is 455 kHz ± 1 Hz then adjust the tuning slug of L4 as necessary for a multimeter indication of 8 ± 0.5 Volts.

(9) Select BFO and tune the BFO using the front panel control. Observe that the frequency meter agrees with the front panel indications.

(10) Typical frequencies, signal levels and voltages as they should be at various test points are shown below. When measuring at TP2 and J1, set INT/EXT switch to INT and ensure links LK1 and LK2 are connected for 1 MHz I/O at J1.

| Test Point | Frequency | Volts | Remarks |
|---|---|---|---|
| TP2 | 5 MHz | TTL | Use Oscilloscope |
| TP5 | DC | 6-11 V | Use multimeter |
| TP8 | DC | 8 ±2 V | Use multimeter |
| TP9 | 22.75 MHz | 300 mV min p-p | Use oscilloscope (BFO set to 0.00 kHz) |
| TP10 | 5 MHz | 1 V min p-p | Use oscilloscope |
| J1 | 1 MHz | 222 mV min | Use RF voltmeter |
| J2 | 1 MHz | TTL | Use oscilloscope |
| J4 | 455 kHz | 0.7 V p-p | Use oscilloscope |

ALIGNMENT PROCEDURE - 1st LO SYNTHESIZER A7

11. Test equipment required: Digital Multimeter, item 1 Table 13-1, Oscilloscope with X1 probe: item 2, Digital Frequency Meter, item 5.

Procedure

12. (1) Connect the digital multimeter between TP1 and ground.

(2) Set R7 for a multimeter indication of 5.2 ±0.01 Volts.

(3) Connect the multimeter between TP16 and ground.

(4) Tune the receiver to 29.99999 MHz, and adjust L11 for a multimeter indication of 15.0 V ± 0.1 V.

(5) Tune the receiver to 00.00000 MHz and ensure that the multimeter indication is not less than 2.5 V.

(6) Set Rx to 15.546 MHz, AM, 6 kHz BW connect oscilloscope AC coupled, sensitivity 5 mV/div 2 µs sweep between TP16 and ground trigger oscilloscope from signal on TP5.
Connect TP7 to ground (TP3).

(7) Adjust R43 for minimum trace amplitude.

(8) Connect the digital frequency meter to 1st LO output at A7 J3.

(9) Observe that the indicated frequency is equal to the receiver tuned frequency plus 40.455 MHz (± instrument error) over the full receiver tuning range.

(10) Disconnect all test equipment and re-connect all module interconnections.

ALIGNMENT PROCEDURE - MICROCOMPUTER A6A2

13. No adjustments are provided on the A6A2 module and alignment is not required. A6A2 clock frequency is 2 MHz nominal.

ALIGNMENT PROCEDURE - IF/AF BOARD A4

14. Test equipment required: Digital Multimeter, item 1 of Table 13-1, RF Voltmeter item 3, Audio Power Meter, item 4, Digital Frequency Meter, item 5, Signal Generator, item 6 and 50 ohm terminating coupler, item 7.

Procedure

15. (1) Connect the Digital Multimeter between TP9 and ground and select AGC SHORT on the front panel of the receiver. With no signal at antenna input adjust R119 for a multimeter reading of 10 volts ±0.05 Volts.

(2) Set the AGC to MAN and turn the IF GAIN control fully clockwise. Select CW BW5 (16 kHz).

(3) Connect the signal generator output to A4J1. Set the signal generator to 455.00 kHz and the output level to 250 µV pd.

(4) Connect the RF voltmeter with 50 ohm termination to the IF OUT socket, J2 on the rear panel.

(5) Adjust L1 and L2 for maximum indication on the RF voltmeter.

(6) Connect the RF Voltmeter, using the high impedance probe, to A4TP7.

(7) With IF GAIN at maximum, bandwidth to 3 kHz, adjust R39 on the A4 board for an indicated 300 mV rms ± dB on the RF voltmeter.

(8) Set the AGC to SHORT. Increase the signal generator level by 35 dB and adjust R47 for 8.5 V ±0.05 V on TP9 measured with the digital multimeter.

(9) Connect the RF Voltmeter to the rear panel IF OUT socket, J2. Select AGC MAN, 6 kHz BW. Adjust the IF GAIN control for 100 mV on the RF voltmeter.

(10) Select each bandpass filter in turn and verify that the required 6 dB bandwidths are obtained by tuning the signal generator through the receiver pass-band.

6 dB BW (min)

| | | |
|---|---|---|
| BW1 | 0.3 kHz | |
| BW2 | 1.0 kHz | |
| BW3 | 3.2 kHz | |
| BW4 | 6.0 kHz | |
| | USB/LSB | -6 dB max, 250 Hz to 3.2 kHz in wanted sideband. |
| BW5 | 16 kHz | |

NOTE: 1 LSB should be measured at A5J3 if ISB IF (A5) is fitted.

2 The 6 dB bandwidths may differ from those listed above if optional filters are fitted.

(11) Connect the audio power meter, set to 600 ohms, to the MONITOR LINE OUT, pins 4 and 17 of J3 on the rear panel.

(12) Set the receiver AGC to SHORT, MODE to CW, BFO 1 kHz offset.

(13) Connect the signal generator to the A4 IF input using the BNC adaptor.

(14) Set the signal generator to 455 kHz CW output at a level of 10 mV pd.

(15) Adjust AF LINE LEVEL preset control R129 on A4 for 1 mW output. (.775 V in 600 ohms).

(16) Select AM mode and 6 kHz bandwidth.

(17) Connect the audio voltmeter to LINE OUT pins 1 and 14 on J3 on the rear panel. Modulate the signal generator to 30 % at 1 kHz and check for audio output indication on the Audio Voltmeter.

(18) Select FM mode and 16 kHz bandwidth.

(19) Modulate the signal generator frequency at a 1 kHz rate with a peak deviation of 5.6 kHz.

(20) Peak L3 for maximum AF output.

(21) Connect the output power meter set to 15 Ω to the output terminals of J3.

(22) Set the VOLUME control on the front panel to maximum. Ensure that the indicated AF output level is at least 200 mW into 15 ohms.

(23) Disconnect all test equipment, reconnect all removed module interconnections.

ALIGNMENT PROCEDURE ISB IF/AF A5

16. The circuits employed in A5 are identical to the relevant circuits of A4. Refer to the alignment procedures of A4 for realignment of this module.

ALIGNMENT PROCEDURE 2nd MIXER A3

17. Test equipment required: Digital multimeter, item 1 of Table 13-1, Signal Generator, item 6, RF voltmeter, item 3.

Procedure

18. (1) Set the receiver controls for AM reception, 16 kHz bandwidth, AFC manual, and IF GAIN maximum.

(2) Connect the RF voltmeter to the IF OUT connector J2 on the receiver rear panel.

(3) Disconnect P1 from A2J3. Set R24 on the A3 board fully clockwise.

(4) Using the Signal Generator inject a 40.455 MHz signal to P1 and adjust the level to produce an IF output indication of 100 mV rms.

(5) Adjust the following trimmers in the order shown for peak output indication on the RF voltmeter, reducing the signal generator level as required to maintain the 100 mV output reference. Adjust L7, L6, L5, L4 and T1 for peak.

(6) With the signal generator input level of 1 μV emf at the A3 input, the signal plus noise to noise ratio at the audio output in a 3 kHz bandwidth should be at least 18 dB.

(7) Remove all test equipment and re-instate all module connections.

ALIGNMENT PROCEDURE - 1st MIXER MODULE A2

19. Test equipment required: RF Voltmeter, item 3 of Table 13-1 and Signal Generator, item 6.

Procedure

20. (1) Remove the local oscillator input to J1 of A2.

(2) Connect the signal generator to the LO input A2J1. Set the output to 0 dBm.

(3) Connect the RF voltmeter using the high impedance probe to TP2 of A2.

(4) Set the receiver front panel controls to AM mode, AGC MAN, 16 kHz BW and IF GAIN to maximum.

(5) Turn SUPPLY switch to ON.

(6) Tune the signal generator to 17.6 MHz. Adjust coil L3 of A2 to provide a notch (minimum amplitude) at 17.6 MHz while observing the RF voltmeter indication.

(7) Tune the signal generator to 26.045 MHz. Adjust coil L4 in the same manner except to provide a notch at 26.045 MHz.

(8) Disconnect the signal genertor from J1 and connect it to P1 (RF INPUT).

(9) Connect the RF voltmeter with the high impedance probe to the links between E3 and E5.

(10) Set the generator to 50.2 MHz. Adjust L5 for minimum level indication on the RF voltmeter.

(11) Set the generator to 40.45 MHz. Adjust L2 for minimum level indication on the RF voltmeter.

(12) Reconnect input cable P1 to chassis. Reconnect the LO input to J1.

(13) Set the receiver frequency to 2.00000 MHz.

(14) Connect the output of the signal generator to the chassis-mounted first mixer input coax connector. Set the signal generator frequency to 2.000 MHz and output level to 1 μV emf.

(15) Connect the RF voltmeter, with the 50 ohms input impedance adaptor, to the IF OUT connector, J2 on the rear panel. Select CW, 3 kHz bandwidth, MAN. Turn IF GAIN control fully clockwise.

(16) Tune the signal generator to maximum output, as indicated on the RF voltmeter. Tune T5 for maximum output.

(17) With the signal generator input level of 1 µV emf at the A2 input the signal plus noise to noise ratio at the audio output in a 3 kHz bandwidth should be at least 10 dB at frequencies between 500 kHz and 30 MHz.

(18) Set the receiver supply switch to off. Disconnect all test equipment. Reinstate all module connections.

ALIGNMENT PROCEDURE - RF AMPLIFIER/LOWPASS FILTER A1

21. Signal generator, item 6; RF voltmeter, item 3.

NOTE: Do not attempt to align the four-section low pass filter without a spectrum analyser/tracking generator.

Procedure

22. (1) Connect the signal generator to the antenna input socket A1J1 and the RF voltmeter with 50 ohm termination to the RF out connector W2P1. Set the signal generator level to -10 dBm.

(2) If the RF amplifier is linked out ensure that the loss through the A1 module does not exceed 1.5 dB from 500 kHz to 30 MHz.

(3) If the RF amplifier is linked in ensure that the gain through the A1 module is 8 dB ± 2 dB from 500 kHz to 30 MHz.

(4) Reconnect W2P1 to chassis connector J5.

(5) With a signal generator input level of 1 µV emf at the A1 input the signal plus noise to noise ratio at the audio output in a 3 kHz bandwidth should be at least 10 dB with the RF amplifier linked out and at least 15 dB with it linked in.

ALIGNMENT PROCEDURE - FRONT PANEL MODULES A9A1 and A9A2

23. Oscilloscope Dual Trace item 2

Connect oscilloscope, DC coupled, to TP15 and TP16 in turn. Adjust R50 and R51 respectively to obtain a square waveform as shown below in Fig 13.3.

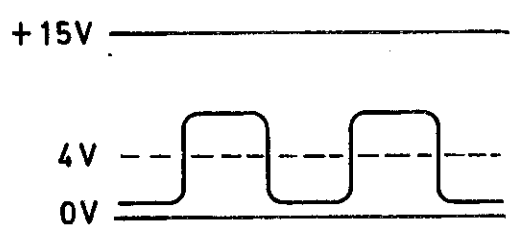



**Fig 13.3**
**Sensor Setting Waveform**

## FINAL GAIN AND AGC ADJUSTMENTS

24. Following the adjustment or replacement of the A1, A2, A3, A4 or A5 modules the following gain and agc adjustments should be made.

(1) Connect the signal generator to the antenna input A1J1 and set the frequency to 1.02 MHz.

(2) Connect the audio power meter to the MONITOR line output, J3 pins 4 and 17. Connect the dvm to DIV AGC output, J3, pins 21 and 9. Set R105 on A4 fully clockwise.

(3) Set the receiver to USB, agc short and tune it to the signal generator. Set the signal generator level to 60 µV emf. Adjust R129 on A4 for 0 dBm output on the power meter.

(4) Reduce signal generator level to 1 µV emf, select MAN. and IF GAIN fully clockwise and adjust R39 on A4 for 0 dBm on the power meter.

(5) Select AGC SHORT and increase the signal generator level to 60 µV emf. Adjust R47 on A4 for an indication of 8.5 ± 0.05 on the dvm.

(6) Connect the RF voltmeter with high impedance probe to TP1 on A4 board. Note the level on the RF voltmeter and slowly turn R105 on A4 anti-clockwise until this level is reduced by 1 dB.

25. If the receiver is fitted with the ISB option the following adjustments should be made.

(1) Connect the dvm to the ISB DIV AGC output, J3 pins 22 and 9.

(2) Set the receiver to LSB, AGC SHORT and tune to the signal generator. Set the signal output level to 60 µV emf. Adjust R132 on A4 for 0 dBm output on the power meter.

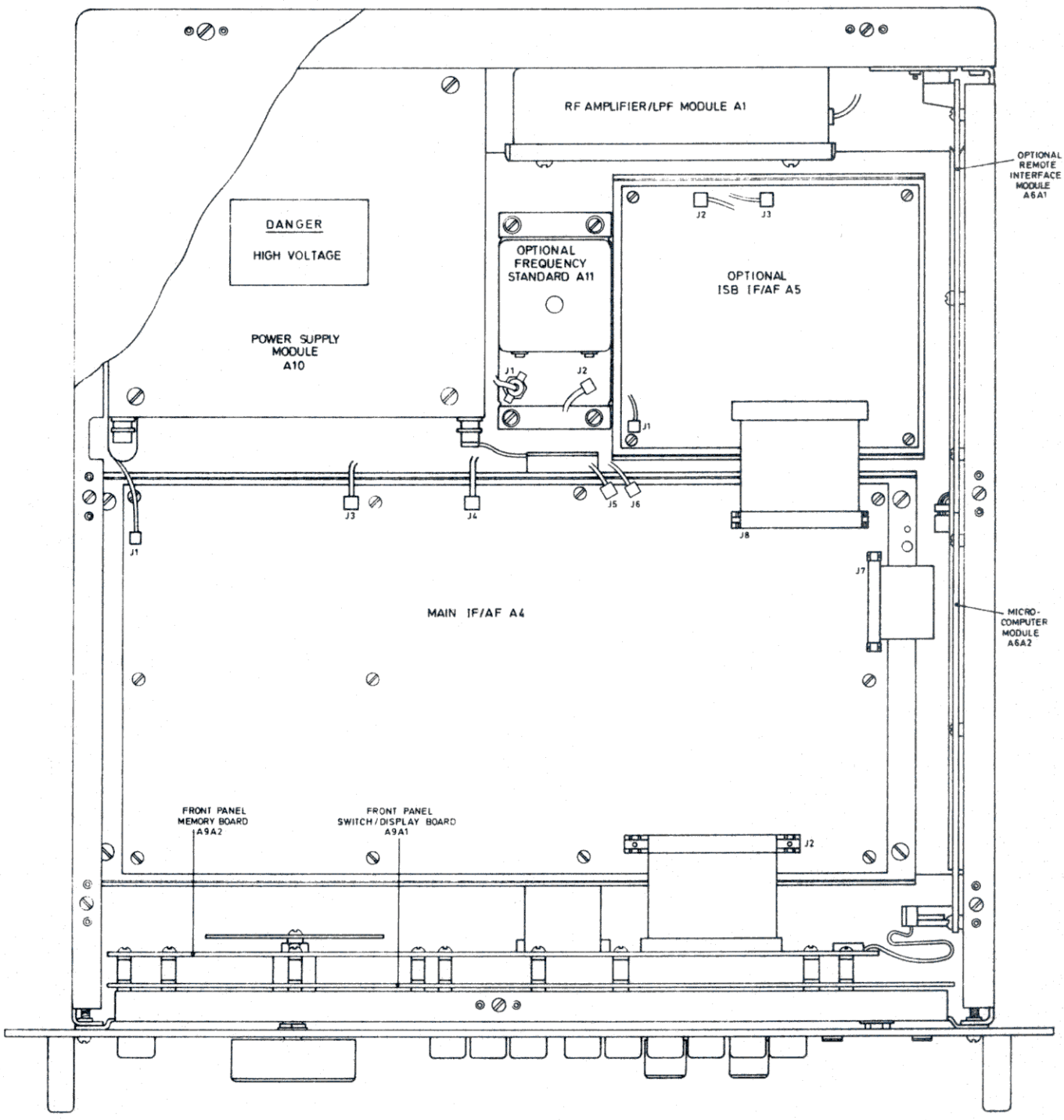
(3) Reduce the signal generator level to 1 µV emf, select MAN. and set the IF GAIN control fully clockwise. Adjust R19 on A5 for 0 dBm on the power meter.

(4) Select AGC SHORT and increse the signal generator level to 60 µV emf. Adjust R23 on A5 for an indication of 8.5 ± 0.05 V on the dvm.

Table 13-1

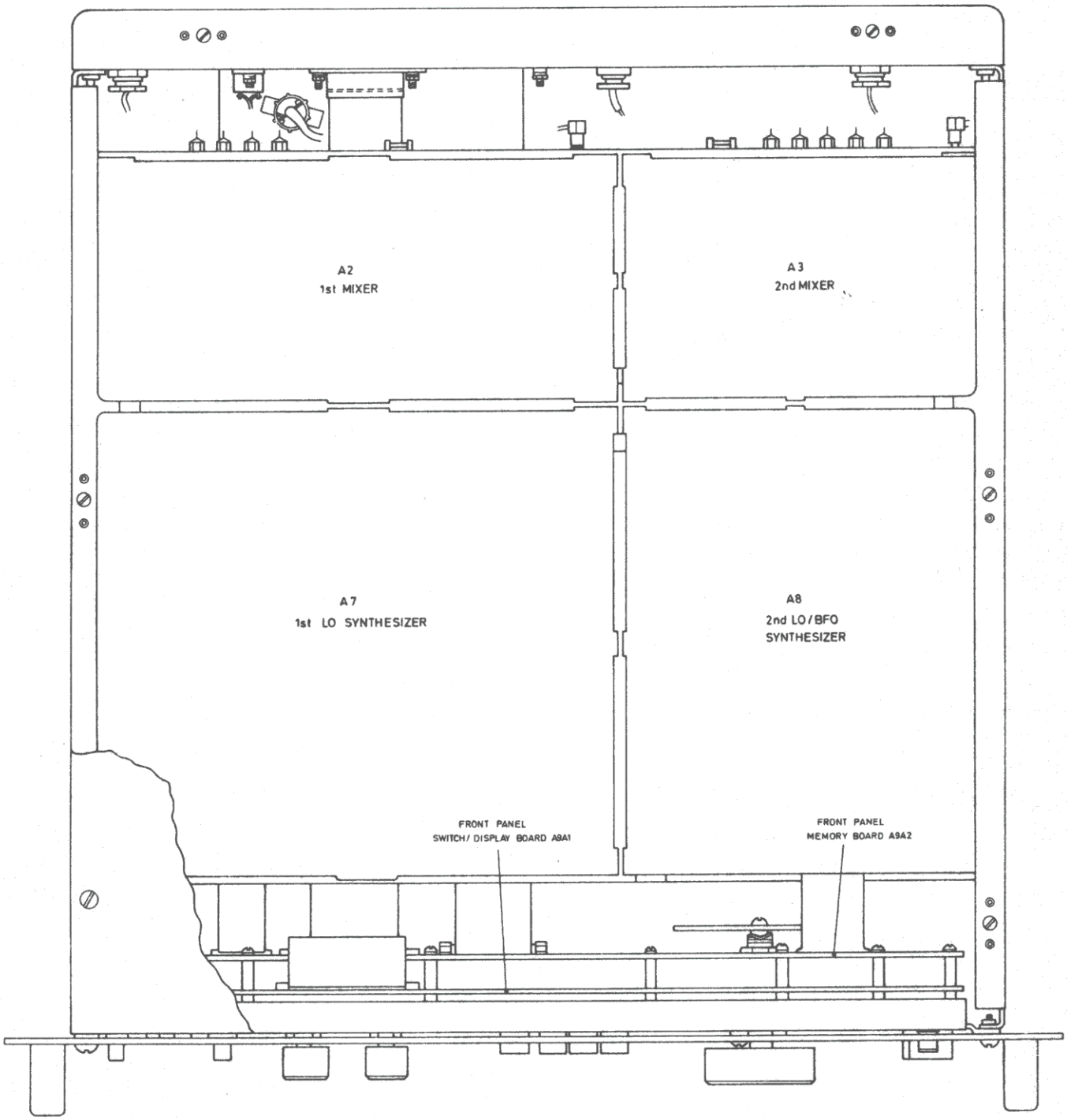
TEST EQUIPMENT

| Item | Instrument | Specification | Recommended Instrument |
|---|---|---|---|
| 1 | Digital Multimeter | Range: 0 to 150 V ac and dc<br>0 to 1 A ac and dc<br>Display: 3½ digits<br>Accuracy: ±3% | Racal 4002 |
| 2 | Oscilloscope, Dual Trace | Sensitivity: 5 mV/div.<br>Frequency: dc to 2 MHz | Tektronix 465 |
| 3 | RF Voltmeter | Range: 300 mV to 3 V rms<br>Frequency: 100 kHz to 70 MHz<br>Input Impedance: 1 Mohm with 50 ohm adaptor<br>Accuracy: ±1% of full scale | Racal 9301A |
| 4 | Audio output power meter | 1 mW - 1 W<br>15 Ω and 600 Ω | Marconi TF893B |
| 5 | Digital Frequency Meter | Frequency Range: 0 to 50 MHz<br>Sensitivity: 10 mV rms<br>Impedance: 1 Mohm<br>Accuracy: 1 part in $10^6$ ±1 count | Racal 9904 |
| 6 | Signal Generator | Frequency Range: 450 kHz to 50 MHz<br>Accuracy and Stability: Output frequency is locked to the frequency standard in use.<br>Output Level Range: -130 dBm to +13 dBm into 50 Ω.<br>Modulation: AM 800 mV into 600 Ω gives 80% mod. depth.<br>FM 1 V into 600 Ω gives peak selected deviation. Peak deviation is between 10 kHz and 300 kHz depending on selected range.<br>Output Impedance: 50 Ω | Racal 9084 |
| 7 | Terminating Coupler | 50-ohm BNC-SMB | |




Top View: RA.1792 Receiver

Fig.13.1




Bottom View RA.1792 Receiver

Fig.13.2

# CHAPTER 14

# FAULT FINDING PROCEDURES

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* Signature analysis for the A6A2 Processor Board (ROM) depends upon the software number.

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# CHAPTER 14

# FAULT FINDING PROCEDURES

## INTRODUCTION

1. This chapter details fault-finding procedures for the RA 1792 HF Communications Receiver. Tests have been provided to diagnose a faulty receiver and to locate the faulty module/board.

2. Provision has been made for two separate methods of fault-finding to be used. The methods may overlap to some extent, but in general provide fault indication in the areas specified:-

   (1) BITE (Built-In Test Equipment)

   This may be regarded as the first step in checking receiver status. The microcomputer (A6A2) performs a sequence of tests, the failure of any test being indicated on the front panel displays. Table 14-3 lists BITE tests and failure indication shown.

   (2) Signature Analysis

   This technique permits a unique 'signature' to be realised for any part of the receiver logic system. Comparison with the relevant tables (14-5 to 14-12) allows the engineer to identify faulty operation in the section of circuitry whose signature is being checked. Signature Analysis is particularly effective in tracing faults in the microprocessor area.

3. Paragraphs 10 and 11 describe switch-on procedures and simple operation checks. If an obvious fault is not revealed during these checks, then BITE should be used next. If specified performance cannot be obtained, or if BITE indicates a fault, then either the Signature Analysis tests or the Flow-Chart method must be used.

4. Refer to the appropriate chapters in this manual for circuit description of the module under test. A circuit diagram will be found at the end of each chapter.

5. A certain amount of dismantling is necessary to gain access to certain modules in the receiver. Procedures for dismantling and re-assembly are contained in Chapter 13, para 6. Following repair and subsequent re-alignment where necessary (refer to Chapter 13 for Alignment procedures), ensure that all dismantled assemblies are correctly re-assembled and that all covers are replaced.

6. For operating instructions, refer to RA 1792/MA 1075 Operators Manual.

## SAFETY PRECAUTIONS

7. Observe all safety regulations. Do not replace modules or make adjustments (except when aligning trimmers or other adjustable components) with power applied to the receiver.

WARNING

Voltages within this equipment are sufficiently high to endanger life. Use caution when servicing power supplies or their load components.

## EQUIPMENT REQUIRED

### List of Test Equipment

8. Table 14.1 is a list of test equipment recommended for conducting fault-finding and maintenance procedures. Alternative test equipment of similar specification may be used.

### Special Tools

9. No special tools other than normal hand tools are required for the replacement of any module in the RA 1792 receiver.

## SWITCH-ON PROCEDURE AND OPERATIONAL CHECKS

10. The following procedure is useful as a first step to fault-finding by identifying possible faulty operation of the receiver.

NOTE: Preset parameters may be corrupted after long periods of non-use if battery discharges. See Chapter 10 Page 10-12 para 29 for Preset Mode Procedure.

### Procedure

11. (1) Inspect the equipment for signs of physical damage.

(2) Check all controls for correct mechanical action, i.e. freedom from binding, scraping or general interference of parts.

(3) Set REF INT/EXT switch (S2) on rear panel to INT unless an internal frequency standard is not fitted.

(4) Ensure that the rear-panel voltage selector is correctly set to suit the source of supply.

(5) Connect the receiver to the local source of supply.

(6) Connect a pair of headphones to the front panel PHONES socket.

(7) Set the POWER switch on the RA 1792 Receiver to ON.

(8) Ensure that the front panel displays are activated after a delay of approximately one second.

(9) Select each control function in turn by pressing the appropriate switches (refer to RA 1792/MA 1075 Operators Manual for operating procedures) and observe that the front panel displays indicate that the correct function has been selected and that the tuned and BFO frequencies are correctly displayed.

(10) Select 16 KHz bandwidth, AM detector, Manual IF gain and enter a frequency above 500 kHz. Obnserve that the noise output from the receiver varies with the setting of the IF GAIN and VOLUME controls, becoming louder as the controls are advanced.

(11) Select SHORT AGC. Select each bandwidth in turn and observe that the receiver noise level falls as the bandwidth is reduced.

Table 14.1 TEST EQUIPMENT

| Item | Instrument | Specification | | Recommended Instrument |
|---|---|---|---|---|
| 1 | Signal Generator | Frequency Range: | 450 kHz to 50 MHz | Racal 9084 |
| | | Accuracy and Stability: | Output frequency is locked to the frequency standard in use | |
| | | Output Level Range: | -130 dBm to +13 dBm into 50Ω | |
| | | Modulation: | AM 800 mV into 600Ω gives 80% mod. depth FM 1 V into 600Ω gives peak selected deviation. Peak deviation is between 10 kHz and 300 kHz depending on selected range. | |
| | | Output Impedance: | 50Ω | |
| 2 | Digital Frequency Meter | Frequency Range: | 0 to 120 MHz | Racal 9912 |
| | | Sensitivity: | 10 mV r.m.s. | |
| | | Impedance: | 1 Mohm | |
| | | Accuracy: | 1 part in $10^6$ ±1 count | |
| 3 | Oscilloscope, Dual Trace | Sensitivity: | 5 mV/div. | Tektronix 465 |
| | | Frequency: | d.c. to 2 MHz | |
| 4 | RF Voltmeter | Range: | 300 mV to 3 V r.m.s. | Racal 9310A |
| | | Frequency: | 100 kHz to 70 MHz | |
| | | Input Impedance: | 1 Mohm with 50 ohm adaptor | |
| | | Accuracy: | ±1% of full scale | |
| 5 | Digital Multimeter | Range: | 0 to 150 V a.c. and d.c.<br>0 to 1 A a.c. and d.c. | Racal 4002 |
| | | Display: | 4½ digits | |
| | | Accuracy: | ±3% | |
| 6 | Audio Output Power Meter | 1 mW - 1 W<br>15Ω and 600Ω | | Marconi TF893B |
| 7 | Signature Analyser | | | HP5006A |
| 8 | Score Loopback Connector | | | ST863 |

(12) Select FM then CW and observe that the character of the noise output changes for each demodulator.

(13) Select MEDIUM AGC, enter tuned frequency 0 MHz, select BFO tune and tune the BFO through the range -8 kHz to +8 kHz. Observe that a beat note corresponding to the BFO offset is audible.

(14) Tune the BFO to + 1.00 kHz, and observe that RF and AF levels are indicated as appropriate on the LCD meter scales.

(15) Connect an antenna to the rear panel antenna socket and tune to a known transmission. Refer to Operator's Manual and observe that all controls function normally.

## BITE FAULT LOCATION

### Sticking Switches

12. BITE provides an automatic test for the front-panel push-button switches when power is first applied. The test checks for sticking switches, and if this is the case, gives the number of the sticking switch on the front panel display in the first two digits of the frequency readout.

Refer to Table 14.2 for pushbutton reference numbers.

TABLE 14.2 FRONT PANEL PUSHBUTTONS

| FRONT PANEL PUSHBUTTON REFERENCE NOS. | FRONT PANEL PUSHBUTTON FUNCTIONS | FRONT PANEL PUSHBUTTON REFERENCE NOS. | FRONT PANEL PUSHBUTTON FUNCTIONS |
|---|---|---|---|
| 01 | REM | 014 | 0 AUX |
| 02 | BFO | 015 | ENTER |
| 03 | TUNE | 016 | FREQ |
| 04 | 1BW1 | 017 | CHAN |
| 05 | 2BW2 | 018 | RCL |
| 06 | 3BW3 | 019 | CHAN SCAN |
| 07 | 4BW4 | 020 | ISB |
| 08 | 5BW5 | 021 | LSB |
| 09 | 6 MAN | 022 | USB |
| 010 | 7 SHORT | 023 | AM |
| 011 | 8 MED | 024 | CW |
| 012 | 9 LONG | 025 | FM |
| 013 | STORE | | |

13. If the display indicates that a switch is sticking, proceed as follows:

(1) Inspect the switch panel for physical problems such as distortion and misalignment.

(2) Remove the Front Panel Switch and Display board (see Chapter 13) and using a continuity meter, check for permanently closed switches. If one or more switches are found to be permanently closed then they should be replaced and the Front Panel Switch and Display board refitted and the Receiver re-tested.

(3) If neither of the above steps allow successful completion of the push-button switch test, then the Front Panel Switch and Display board (A9A1) must be replaced.

Manually Selected Tests

14. After the switch test has been completed, BITE is then available for the manually selected series of tests. This comprises a group of 34 tests which are listed in Table 14.3, and described in paragraphs 15-32.

To enter these tests press and hold the 'REM' push-button and then press the start test number '00'. Release the 'REM' push-button and the receiver will automatically execute tests 00 to 29 and wait for manual intervention with test number 30 flashing in the channel number display. This is a prompt to connect the score loop-back connector to A6A1J1 on the rear panel of the receiver. Press 'REM' to continue. Tests 30 to 33 will now be executed leaving the receiver in BITE continuous update mode. This continually strobes data to the synthesizers and displays etc. to update the whole receiver for use in fault finding, and is distinguished from normal running by flashing the REMOTE indicator in the lefthand L.C.D. Press 'RCL' to return to normal running.

The BITE routine may be entered at any test number and if a failure occurs, pressing 'REM' will, in most cases, repeat the failed test.

TABLE 14.3 BITE TESTS

NOTE: The test number is indicated in the channel area of the front panel display. If a test fails, the 'fault' indicator is activated also.

| Test No. | Test Details | Failure Indication |
|---|---|---|
| 0 | PSU + 5 volt line voltage | |
| 1 | PSU + 12 volt line voltage | |
| 2 | PSU + 20 volt line voltage | 'H' or 'L' plus voltage |
| 3 | PSU + 15 volt line voltage | being measured, is shown |
| 4 | PSU - 15 volt line voltage | in the frequency display. |
| 5 | PSU - 30 volt line voltage | |
| 6 | PSU - 12 volt line voltage | |
| 7 | Display test. All display segments switched ON sequentially and then OFF at a reasonably slow rate. | Visually note any segments which fail. |
| 8 | ROM sumcheck | Faulty sumcheck figure |
| 9 | Non-destructuve RAM test | Number of faulty IC shown |
| 10 | Non-destructive EAROM test | Number of faulty IC shown |
| 11 | Reference oscillator varactor line voltage | NOTE: This voltage is checked in BITE and also monitored during normal running. |
| 12 | BFO varactor line voltage | Test No + 'fault' indicator |
| 13 | L.O. Synthesizer varactor and voltage sweep test | Test No + 'fault' indicator |
| 14 | A3 AGC line voltage test | Test No + 'fault' indicator |
| 15 | BFO sweep test | Test No + 'fault' indicator |

TABLE 14.3 CONT

| Test No. | Test Details | Failure indication |
|---|---|---|
| | Main IF AGC/MGC Compatibility Tests | |
| 16 | Initial audio level out of range | Test No + 'fault' indicator |
| 17 | Audio level after gain change out of range | Test No + 'fault' indicator |
| 18 | Insufficient isolation by filters | Test No + 'fault' indicator |
| | ISB IF AGC/MGC Compatibility Tests | |
| 19 | Initial audio level out of range | Test No + 'fault' indicator |
| 20 | Audio level after gain change out of range | Test No + 'fault' indicator |
| 21 | Filter insertion loss - filter 1 | Test No + 'fault' indicator |
| 22 | filter 2 | Test No + 'fault' indicator |
| 23 | (GB option only) filter 3 | Test No + 'fault' indicator |
| 24 | Filter insertion loss - filter 4 | Test No + 'fault' indicator |
| 25 | filter 5 | Test No + 'fault' indicator |
| 26 | General fault - all filters low | Test No + 'fault' indicator |
| 27 | AM detector test | Test No + 'fault' indicator |
| 28 | FM detector test | Test No + 'fault' indicator |
| 29 | Flashes 30 as next test. Prompt to connect loopback connector if SCORE board is fitted. | |
| | SCORE Loopback Tests | |
| 30 | SCORE user function port faulty | 01 shown on display |
| 31 | Transmit interrupts faulty | 02 shown on display |
| 32 | Receive interrupts faulty | 04 shown on display |
| 33 | Received data incorrect | 08 shown on display |

DESCRIPTION OF BITE MANUALLY SELECTED TESTS

Power Supply Unit Tests: 0 - 6

15. By the use of additional hardware, this test measures the following voltages:

| | |
|---|---|
| +5V | -15V |
| +12V | -30V |
| +20V | -12V |
| +15V | |

Also, the following:

| | |
|---|---|
| BFO varactor line voltage | (test 12) |
| Reference oscillator line voltage | (test 11) |
| A3 AGC line voltage | (test 14) |

(3) If neither of the above steps allow successful completion of the push-button switch test, then the Front Panel Switch and Display board (A9A1) must be replaced.

Manually Selected Tests

14. After the switch test has been completed, BITE is then available for the manually selected series of tests. This comprises a group of 34 tests which are listed in Table 14.3, and described in paragraphs 15-32.

To enter these tests press and hold the 'REM' push-button and then press the start test number '00'. Release the 'REM' push-button and the receiver will automatically execute tests 00 to 29 and wait for manual intervention with test number 30 flashing in the channel number display. This is a prompt to connect the score loop-back connector to A6A1J1 on the rear panel of the receiver. Press 'REM' to continue. Tests 30 to 33 will now be executed leaving the receiver in BITE continuous update mode. This continually strobes data to the synthesizers and displays etc. to update the whole receiver for use in fault finding, and is distinguished from normal running by flashing the REMOTE indicator in the lefthand L.C.D. Press 'RCL' to return to normal running.

The BITE routine may be entered at any test number and if a failure occurs, pressing 'REM' will, in most cases, repeat the failed test.

TABLE 14.3 BITE TESTS

NOTE: The test number is indicated in the channel area of the front panel display. If a test fails, the 'fault' indicator is activated also.

| Test No. | Test Details | Failure Indication |
|---|---|---|
| 0 | PSU + 5 volt line voltage | |
| 1 | PSU + 12 volt line voltage | |
| 2 | PSU + 20 volt line voltage | 'H' or 'L' plus voltage |
| 3 | PSU + 15 volt line voltage | being measured, is shown |
| 4 | PSU - 15 volt line voltage | in the frequency display. |
| 5 | PSU - 30 volt line voltage | |
| 6 | PSU - 12 volt line voltage | |
| 7 | Display test. All display segments switched ON sequentially and then OFF at a reasonably slow rate. | Visually note any segments which fail. |
| 8 | ROM sumcheck | Faulty sumcheck figure |
| 9 | Non-destructuve RAM test | Number of faulty IC shown |
| 10 | Non-destructive EAROM test | Number of faulty IC shown |
| 11 | Reference oscillator varactor line voltage | NOTE: This voltage is checked in BITE and also monitored during normal running. |
| 12 | BFO varactor line voltage | Test No + 'fault' indicator |
| 13 | L.O. Synthesizer varactor and voltage sweep test | Test No + 'fault' indicator |
| 14 | A3 AGC line voltage test | Test No + 'fault' indicator |
| 15 | BFO sweep test | Test No + 'fault' indicator |

TABLE 14.3 CONT

| Test No. | Test Details | Failure indication |
|---|---|---|
| | Main IF AGC/MGC Compatibility Tests | |
| 16 | Initial audio level out of range | Test No + 'fault' indicator |
| 17 | Audio level after gain change out of range | Test No + 'fault' indicator |
| 18 | Insufficient isolation by filters | Test No + 'fault' indicator |
| | ISB IF AGC/MGC Compatibility Tests | |
| 19 | Initial audio level out of range | Test No + 'fault' indicator |
| 20 | Audio level after gain change out of range | Test No + 'fault' indicator |
| 21 | Filter insertion loss - filter 1 | Test No + 'fault' indicator |
| 22 | filter 2 | Test No + 'fault' indicator |
| 23 | (GB option only) filter 3 | Test No + 'fault' indicator |
| 24 | Filter insertion loss - filter 4 | Test No + 'fault' indicator |
| 25 | filter 5 | Test No + 'fault' indicator |
| 26 | General fault - all filters low | Test No + 'fault' indicator |
| 27 | AM detector test | Test No + 'fault' indicator |
| 28 | FM detector test | Test No + 'fault' indicator |
| 29 | Flashes 30 as next test. Prompt to connect loopback connector if SCORE board is fitted. | |
| | SCORE Loopback Tests | |
| 30 | SCORE user function port faulty | 01 shown on display |
| 31 | Transmit interrupts faulty | 02 shown on display |
| 32 | Receive interrupts faulty | 04 shown on display |
| 33 | Received data incorrect | 08 shown on display |

DESCRIPTION OF BITE MANUALLY SELECTED TESTS

Power Supply Unit Tests: 0 - 6

15. By the use of additional hardware, this test measures the following voltages:

| | |
|---|---|
| +5V | -15V |
| +12V | -30V |
| +20V | -12V |
| +15V | |

Also, the following:

| | |
|---|---|
| BFO varactor line voltage | (test 12) |
| Reference oscillator line voltage | (test 11) |
| A3 AGC line voltage | (test 14) |

If a voltage is found to be out of specification, then the voltage being measured is displayed, together with 'H' (high) or 'L' (low), in the frequency display. In the case of the varactor and AGC lines, a fault is indicated by the test number and the 'fault' legend is displayed.

Display Test : 7

16. The Display test switches on all non-numerics, followed by each numeric set to '8', and then all non-numerics are switched off, followed by blanking each numeric in sequence. This is performed sufficiently slowly to allow observation of faulty numeric and non-numeric displays.

ROM Sum-Check : 8

17. BITE check-sums each ROM. If the specified checksum for a ROM does not agree with the one calculated by this test, then the PD number of the faulty ROM is shown in the frequency display.

RAM Test : 9

18. This test checks the RAM without corrupting any stored data, by writing patterns of '1' and '0' to all bit positions in 4 bytes of RAM. The patterns are then read and should equal those written. If a RAM I.C. fails, its ML number is shown in the frequency display.

EAROM Test : 10

19. This BITE test checks the EAROM without corrupting any stored data, by writing patterns of '1' and '0' to the 8 bytes comprising channel 103, and checking that data read back from these locations is the same as that written. Should either EAROM fail, its ML number is shown in the frequency display.

Reference Oscillator : 11 (see para 15)

20. This is checked at the same time as the supply voltages, when the varactor voltage is checked to be within two preset limits. Operation of the reference oscillator is also automatically checked during normal receiver use.

BFO Varactor Line Voltage : 12 (see para 15)

Local Oscillator Synthesizer Varactor Voltage Sweep Test : 13

21. This test is run in two sections. The first section measures the varactor voltage, checking that it lies between two preset limits, and then steps the synthesizer in 1 MHz steps over the range 41 MHz to 71 MHz, checking for a monotonic increase or decrease (depending on 'mark' of synthesizer) of varactor line voltage. At the end of the first test the varactor voltage is again checked to be within limits.

22. The second part of the test steps the synthesizer in 20 kHz steps. The frequency change issues a pulse to the varactor, after which it settles to a new steady voltage level. The pulse is first verified (direction) and then measured for width between two fixed points. The width of the pulse indicates the amount of voltage change.

23. During normal receiver operation, the synthesizer is automatically checked for the 'in-lock' condition. The varactor line voltage is also checked to be between preset limits.

A3 AGC Line Voltage : 14 (see para 15)

BFO Sweep Test : 15

24. This test steps the receiver and the BFO alternately, first, in 10 Hz steps, then 100 Hz steps, and finally in 1 kHz steps, giving a series of audio voltages when the receiver and BFO are on the same and different frequencies. This test runs up to 10 kHz.

Main IF AGC/MGC Compatability Tests : 16, 17, 18

25. The receiver is set to - 1 kHz (display shows 99.999 MHz), USB, Short and FL7 (B.W = 16 kHz). The audio level is measured and the DAC voltage checked to be between 3.5 and 9.0V. The DAC then measures the AGC voltage and using the remote manual gain facility, manual gain is used to force the AGC line to the voltage previously measured. The audio level is then checked and must be within $\pm$ 2dB of the level measured in test 16. The manual gain voltage is increased by 2.5V to give a gain increase of approximately 60dB. With no filter selected, the audio level is checked to ensure that it is below - 2dBm.

ISB IF AGC/MGC Compatability Tests : 19,20

26. These tests will take place only if an ISB IF/AF module (A5) has been fitted to the receiver. In such cases the tests described in paragraphs 25 are performed, with the exception of the last part : Gain increase of 60dB and no filter selected.

IF Filter Test : 21 - 25, 26

27. This BITE test uses the DAC and the remote manual gain facility to give an audio level equivalent to -2dBm on the Audio Meter scale, with the narrowest-band filter (FL3) selected. The audio level is stored and each of the other filters are switched in (FL4, 6 and 7) and the relevant audio levels are stored. The maximum of all five levels is chosen, and the levels of the other 4 filters checked to ensure that they are within 6 dB of the maximum level.

AM Detector Test : 27

28. The receiver is set to 0.00 MHz (this simulates an unmodulated carrier), with FL7 chosen (16 kHz bandwidth), AM mode, manual gain. This routine tests the demodulator by varying the manual gain control via the DAC to create approximately 30% modulation at approximately 1 kHz. The resulting audio signal is demodulated and the output voltage checked to be within preset limits.

FM Detector Test : 28

29. The receiver is set up to 0.00 MHz. This sets the synthesizer to a nominal 40.455 MHz. In this way a carrier is simulated. Other receiver settings are : short AGC and 16 kHz filter in the FM mode. The detector is tested by swinging the synthesizer by 5 kHz on either side of zero nominal frequency (a total deviation of 10 kHz) to produce an FM signal whose demodulated audio level is tested to be within preset limits.

SCORE Loopback Connector : 29

30. This is a prompt, rather than a test. It warns the operator to connect the SCORE loopback connector if a SCORE board has been fitted to the receiver. The number 30 is continually flashed in the channel readout on the receiver and BITE waits until either RCL is pressed, exiting the test sequence and returning to normal operation, or the SCORE loopback connector is fitted, REM is pressed, at which point the tests continue at No. 30.

SCORE Loopback Tests : 30 - 33

31. Assuming that a SCORE board is present, data is output continuously and the board is checked for output interrupts. The data is read back via the loopback adapter (inserted by the operator in para 30) and the board is checked for input interrupts. Finally, the actual data read back is checked to ensure that it is identical to that sent. During this group of tests the frequency display shows 01020408, indicating that the tests have been successfully concluded.

32. At this point the BITE leaves the automatic test sequence and enters a subroutine which continuously updates the I/O ports until either the RCL button is pressed, returning the receiver to normal operation, or the power is removed from the receiver.

NOTE: If power is removed from the receiver, it will always be set for normal operation when power is restored, even though the receiver may have been running BITE when power was removed.

ADDITIONAL BITE ROUTINES

33. There are three additional routines under BITE which may be selected by operation of SA, a 4-pole switch mounted on the microcomputer board A6A2. The automatic test noted in para 32 may be selected, plus two others. Two LED's indicate the state of SA by being off, flashing or on continuously. Table 14.3 shows the positions of SA, plus the corresponding states of LED's CR1 and CR2, and which routine is running.

Table 14.4 : SA Operation

| SA | | | | LED STATE | | ROUTINE RUNNING |
|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | CR1 | CR2 | |
| OFF | OFF | OFF | OFF | ON | ON | Normal Receiver Operation |
| ON | OFF | OFF | OFF | FLASHING | FLASHING | ROM Signature Analysis |
| OFF | ON | OFF | OFF | ON | FLASHING | I/O Exercise |
| ON | ON | OFF | OFF | FLASHING | OFF | DAC Ramp Test (Not Signature Analysis) |
| Any Other | | | | FLASHING | ON | Continuous Update Mode |

34. Both the ROM test and the I/O exercise listed in table 14.3 are Signature Analysis tests. These will be covered in the appropriate part of this chapter. The DAC ramp test concerns receiver logic and is given below for reference, when required.

DAC Test

35. The Digital to Analogue Converter (DAC) will be found on the Main IF/AF board (A4).

This program tests the DAC by writing an incrementing sequence of numbers (H'00' to H'FF') to the DAC. This produces a ramp which should be observed on an oscilloscope to determine DAC linearity and continuity of the data bus onto the A4 board. Both DAC linearity and data bus continuity will be shown by equal steps in the ramp.

REMEDIAL ACTION

BITE Flowcharts

36. Chart 1 which will be found at the end of this chapter, illustrates the action required to complete the BITE manually selected tests. In the event of failure of any test, the engineer is directed to a particular paragraph in this chapter, which will detail remedial action. After the fault is repaired the BITE sequence may be re-started to check the effect of the repair.

Possible Processor Failure

37. If BITE tests fail at this point, switch OFF power, remove the output plug from the PSU and check the mains input fuse and plug. Also check that the processor board is plugged firmly into position with all IC's present. Switch power to ON and check for correct voltages at the Power Supply Unit output. Disconnect plugs from the Front Panel Memory Board (A9A2) to the 1st L.O. Synthesizer (A7), 2nd L.O./BFO Synthesizer (A8), Main IF/AF board (A4), RF Amplifier (A1) and first and second mixers (A2, A3). Re-connect the power supply.

38. This leaves only the Front Panel Memory Board, Front Panel Switch and Display board (A9A1) and Microcomputer board (A6A2) connected to the power supply. Switch ON and check the voltages on the microcomputer board. If these are correct re-enter BITE. Tests 0 to 10 can run with the boards noted in this paragraph. If the fault persists then refer to the section on Signature Analysis in this chapter.

One or More Power Supply Voltages Incorrect

39. If BITE tests fail at this point, the display will show a voltage and an 'H' or 'L', indicating that the displayed voltage has been found to be high or low. Unplug the output of the PSU and check the output voltage in question. If the voltage is within specification then unplug all boards listed in para. 37. Attempt to re-run this test. If it still fails then check the A9A1, A9A2 and processor boards. If there are two or more supply line failures, then entering the next test number after a failure, on the front panel push-buttons, will test the remaining lines.

40. Having unplugged all boards except 3, if the fault appears to have cleared, reconnect the other boards one by one, re-running the test each time. This will eliminate the faulty board.

ROM Sumcheck Incorrect

41. A failure at this point indicates that the checksum programmed into the PROM does not agree with the checksum calculated by the BITE software. A number in the frequency display refers to the PD number of the faulty device. To rectify the fault, exchange the faulty PROM with one which is known to be good.

Failed Non-Destructive RAM Test

42. If this test fails then the RAM's have failed their write and immediate read test. The RAM power supply lines should be checked first (pin 22). Re-run this test checking that the correct pulses appear on the chip enables and Read/Write lines. If these are all present and correct, then signature analysis tests (later in this chapter) may be applied before changing the I.C.'s.

Failed Non-Destructive EAROM Test

43. If BITE halts here then the comparison between data written to and immediately read back from the EAROM's does not agree. The 'U' number of the faulty I.C. will be shown in the frequency display. The -30 V and the -12 V supply lines must be correct before erasing and writing to the EAROM's is permitted; these voltages should be checked. Alos, check the following:

(1) Write enables.

(2) Chip enables.

(3) Mode control inputs.

If this test still fails with the above correct, then signature analysis tests should be used.

Reference Varactor Voltage out of Limits (A8 board)

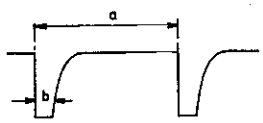
44. If BITE fails at this point, the reference oscillator varactor voltage is outside the preset limits, and may be out of lock. Check which reference source is in use and check that the reference is available at TP1 and TP2. Continue as follows:

(1) Check +15 V and +5 V supplies.

(2) Check on TP3 and TP4 that oscillator is running and is in lock. For correct operation the waveform at each test point should be similar to that shown in Fig. 14.1 (below).

(3) If test still fails, with voltage on TP3 and/or TP4 between 6 V and 11 V, check Q4, Q5, Q6 and U4.

| REFERENCE FREQ. | a | b |
|---|---|---|
| 1 MHz | 1uS | 20nS |
| 5 MHz | 200nS | 20nS |
| 10 MHz | 100nS | 20nS |




Phase Comparator Waveforms Fig.14.1

BFO Varactor Voltage out of Limits (A8 board)

45. Check the following:

(1) Supply voltages to the A8 board.

(2) BFO is set to 0.00 kHz.

(3) Waveforms on TP1 and TP2 (should be similar to those shown in Fig. 14.1, but with a = 2 mS and b = 30 nS.

(4) With BFO set to 0.00 kHz, voltage at TP8 should be 8 V ±0.5 V.

(5) Pin 2 of U21 is at logic '0' (to enable BFO).

(6) TP9 has a signal 300 mV p-p at 22.75 MHz.

Synthesizer Varactor line not showing Monotonic change (A7 board)

46. Check the following:

(1) Correct supply voltages to the A7 board.

(2) The reference frequency.

(3) Voltage should be between 3.5 V and 15.0 V measured on TP19. As reception frequency is increased, voltage on TP9 increases within above limits. If the above checks do not reveal the fault, then signature analysis is necessary.

A3 AGC Voltage out of Limits

47. If BITE fails at this point, place the receiver in the Manual Gain mode and check the voltage at TP14, on the main IF/AF board (A4), which should be greater than 12.5 V for maximum gain, and less than 1.0 V for minimum gain. Check that this voltage is available on the A3 board.

If the synthesizer test has run successfully, the receiver should be set to 0.00 MHz for the present test. Check that the frequency is correctly set. If receiver frequency is correctly set to 0.00 MHz, then an incorrect voltage at TP14 may indicate that U17 is faulty.

48. If the fault persists, check:

(1) A1J1 connector and cables (signal input to A4).

(2) Power to A1 (Input preamplifier/filter).

(3) J1 and J2 on A2 (First mixer board).

(4) Cable linking A8 (Second LO/BFO Synthesizer) to A3. This cable carries the 40 MHz reference.

Audio Levels on Combined Synthesizer/BFO Sweep Tests Outside Limits

49. Perform checks on the A8 board (Second LO/BFO Synthesizer) as follows:

(1) BFO output passing from J4, A8 board to J5, A4 board.

(2) BFO is in lock (assuming test 12 ran correctly). If not, suspect the product detector and the audio section.

(3) Output of U18 (limiting amplifier), pin 10, should show a square wave of 1.2 V p-p.

(4) Signal input to U20 should be approximately 4 V.

(5) Detector Select Switch enable (U19, pin 11) is at logic '0' (thus selecting the product detector).

(6) U19 pin 10 is at logic '0', selecting the output of the audio crosspoint switch for measurement.

(7) A 22.75 MHz signal should be present at TP9.

Initial Audio Voltage out of Range on AGC/MGC Compatibility

50. The following checks should be made on the A4 (Main IF/AF) board:

(1) Display should show 99.999 MHz.

(2) Signal Input Cable is connected to J1.

(3) Signals should be present on TP1, TP6 and TP7.

(4) BFO Cable from A8 to A4 board should be securely connected.

(5) On U20 (Synchronous Detector), check for a carrier input to pin 8 and a signal input to pin 1.

(6) U19 pin 10 should show logic '1' and pin 11 should show logic '0'.

DAC Unable to Set Gain Manually, to Provide an Audio Level Within 2 dB of Original Audio Level

51. The following checks should be made on the A4 board:

(1) Select manual gain (local) and ensure that the gain control operates. Select BITE test 17 and check U11 pin 12 for logic '0', U11 pin 6 for logic '1', and U12 pin 6 for a logic '1'. These conditions should set up remote manual gain using the DAC.

(2) Ensure that U11 pin 13 is at logic '1' (this selects peak-signal gain control).

(3) Check items listed in para 50.

Insufficient Isolation by Filters

52. If BITE stops at this point, then the filters on the A4 board are not isolating the incoming signal sufficiently. This could be faults in the filters themselves, or in the diode switching networks associated with each filter. With the receiver set to normal operation (if this is possible), select each filter in turn and check the voltage at the junctions of CR1 to 7 and CR8 to 14. With a filter selected, the reading should be 7.8 V, and 1.9 V with a filter not selected.

Initial Audio Voltage Out of Range on AGC/MGC Compatibility (ISB IF)

53. With an ISB (AS) board fitted, perform checks as follows:

(1) Link LK1 on A4 board set to the ISB position.

(2) RF cables from J3 and J6 on the A4 board are correctly connected.

(3) Ribbon cable from A4 board correctly connected.

(4) 300 mV RMS signal (ISB IF) at TP7.

(5) 3.0 V p-p sinewave (BFO Carrier) at TP10.

(6) 1.0 V p-p signal (output from U11, synchronous detector) at TP13.

DAC Unable to Set Gain Manually to Provide Audio Level to Within 2 dB of Original Audio Level (ISB AGC)

54. Repeat the checks given in para 51, but on the ISB (A5) board. U9 pins 12 and 13 should be at logic '1', and pin 6 at logic '0'. The logic '1' on pin 13 selects manual gain. If fault persists, repeat on the ISB board, checks given in para 50.

Filter More Than 6 dB below Maximum of all Filters

55. A BITE failure here shows that one of the IF filters shows an insertion loss of more than 6 dB below the reading obtained from the best filter. the last digit of the test number indicates which filter has failed (i.e. 21 indicates Bandwidth 1 = 300 Hz, etc.). Perform checks as follows:

(1) Check that the PROM's installed are correct for the filter option installed.

(2) Check that filters are not missing or damaged and that the correct filters have been fitted.

(3) With the receiver in normal running, select the filter which failed in BITE, and check that the diode isolation network works correctly, with the junction of diodes CR1 to 7 and CR8 to 14 showing 7.8 V with a filter selected, and 1.9 V with a filter not selected.

(4) Set the receiver to 0.00 MHz, BFO at 1 kHz. Listening to the audio tone produced, compare a known 'good' filter with the suspected faulty one. If the signal level on the suspected filter is substantially lower than the 'good' one, then the filter is faulty and should be changed.

56. A failure on test 26 indicates that the IF signal from the A3 (second mixer) board is absent. Check cable connections. The IF signal enters the filters via J1 on the A4 board.

AM Detector Audio Output Level out of Limits

57. The AM detector is located on the A4 (main IF/AF) board. If BITE tests have passed test No. 15 (BFO Sweep test), then it is unlikely that this demodulator is faulty. However, whilst running this test, check as follows:

(1) Input signal should be present at U20, pin 1. Output signal should be present at U20, pin 6 (TP15).

(2) Check that U19, pin 11 is at logic '0' (AM detector selected).

(3) Set the processor DIL-switch to select DAC test (see Table 14.3) to check for DAC linearity.

FM Detector Audio Output Level out of Limits

58. Perform the following checks on the A4 (main IF/AF) board:

(1) Input signal should be present at U18, pin 4. Output signal should be present at U18, pin 1 (TP12).

(2) Check that U19, pin 11 is at logic '1' (FM detector selected).

(3) Set the processor DIL-switch to select DAC test (see Table 14.3) to check for DAC linearity.

SCORE Loopback Test Failure

59. Check that a SCORE board is fitted and plugged fully into the processor board. Select I/O Exercise routine on processor DIL switches and use signature Analyser to check I/O control lines, particularly IOC7, (which is used exclusively for SCORE) on ports 0 and 1 on the processor IC. If these lines show correct signatures, then the fault is likely to be in the SCORE board.

60. Failures in SCORE tests indicate problems in the following areas:

(1) Test 30 indicates faulty user functions.

(2) Test 31 indicates faulty transmit interrupts.

(3) Test 32 indicates faulty receiver interrupts.

(4) Test 33 indicates that data was incorrectly received.

SIGNATURE ANALYSIS

Introduction to Signature Analysis

61. In normal receiver operation the execution of non-sequential program instructions causes continuously changing data patterns throughout the receiver logic circuitry, making data analysis using conventional test equipment (oscilloscopes, logic analysers, etc.) almost impossible.

To overcome this problem a technique called Signature Analysis is employed, in which the microprocessor is forced to continuously execute test routines resulting in continuous repetitive data patterns to be present at data nodes throughout the logic circuitry. These nodes are then examined with the test probe of a signature analyser which identifies the repetitive data patterns by generating a unique signature (4 digit alpha-numeric code) characterising the accumulative data pattern occurring over a specified period of time. The test signatures obtained are then compared with reference signatures (generated from an equipment that is known to be operating correctly). Matching signatures (test and reference) imply that the section of logic that is exercised by the test routine is functioning correctly. If an incorrect signature is obtained, then that particular section of logic is not functioning correctly. The incorrect signatures should then be traced "logically back" through the circuit until an element with correct inputs and faulty output is isolated.

## Fault Location

62. When a fault has been isolated to a Device Under Test (DUT) with correct input signatures and incorrect output signature(s), then the fault will be one of the following (Fig. 14.2):

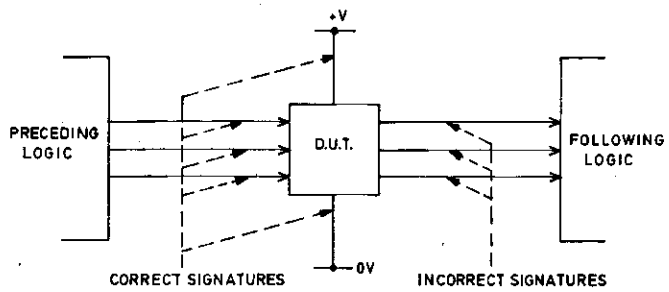
(1) DUT faulty.

(2) DUT output track(s) faulty (short circuits).

(3) DUT output(s) loaded by following logic.

If the output signatures of the preceding logic are correct and the input signature(s) of the DUT are incorrect then suspect a break in the connecting track(s).

If a faulty signature is found to be 0 V (0000) or +V (signature given with test instructions) this can give a guide as to the type of fault present.




Fault Location Fig.14.2

## Using the Signature Analyser

63. Generally, Signature Analysers (e.g. HP 5004, HP 5005) have an integral logic probe which may be used as a test instrument independent from the Signature Analyser. The probe tip lamp indicates the four following conditions at the data node under test:

(1) Probe tip OFF logic 0 (GND)

(2) Probe tip ON logic 1

(3) Probe tip HALF ON High impedance/poor logic level

(4) Probe tip FLASHES(F) Data Stream.

The code shown in brackets is used in the following signature tables to indicate the condition of the probe tip where important.

64. In normal operation, signals applied to the signature analyser initiate (START) and terminate (STOP) a measurement time period (window; gate). A CLOCK input synchronizes and controls the data sample rate of the probe input so that data is input to the Signature Analyser and processed every clock cycle within the START/STOP interval. The START and STOP inputs are individually selectable for logic '1' or '0' levels. The CLOCK input is edge triggered and can be selected for either rising or falling edges. The signature analyser configuration for each set of signatures is given in the following test instructions along with any other conditions which should be met.

65. There are two levels of signature analysis in the RA 1792:

(1) ROM signature analysis which tests the data bus to the memory IC's and checks the contents of the ROM's.

(2) I/O signature analysis which exercises all bits of the I/O control and data buses.

The signatures for the I/O signature analysis are the same for all options of the RA 1792 program, whereas the ROM signatures vary with the program used. It is therefore necessary to check that the correct table of signatures is used when testing the ROM contents.

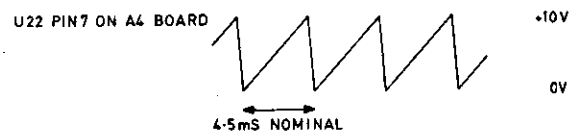
66. To enter the signature analysis modes, select the following switch positions on the DIL switches on the processor board ("ON" = towards bottom of receiver):

| Mode | S1 | S2 | S3 | S4 |
|---|---|---|---|---|
| Normal running | OFF | OFF | OFF | OFF |
| ROM signature analysis | ON | OFF | OFF | OFF |
| I/O signature analysis | OFF | ON | OFF | OFF |
| DAC ramp test | ON | ON | OFF | OFF |
| Normal running | ALL OTHER COMBINATIONS | | | |

When returning to normal running, from a test mode, the receiver is left in BITE continuous update mode. Press RCL to exit from BITE.

DAC Ramp Test

67. This provides a ramp waveform at the output of the D/A converter on the Main IF Board A4. The waveform can be observed with an oscilloscope on pin 7 of U22 and should be as shown in Fig. 14.3:




DAC Ramp Test Fig.14.3

ROM Signature Analysis

68. (1) Connect the signature analyser (Hewlett Packard 5004A) to the following test points on the A6A2 microprocessor board:

(a) START to TP11, trigger on negative edge

(b) STOP to TP11, trigger on positive edge

(c) CLOCK to TP3, trigger on negative edge

(d) GND to TP14

(2) Select the correct switch positions for ROM signature analysis and ensure that both LEDs on the processor board are flashing in synchronisation.

(3) Now check the signature given in Tables 14.5 ensuring that the correct software number appears in the table heading.

I/O Signature Analysis

69. (1) Connect the signature analyser to the following test points on the A6A2 microprocessor board:

(a) START to TP11, trigger on negative edge

(b) STOP to TP11, trigger on positive edge

(c) CLOCK to TP2, trigger on negative edge

(d) GND to TP14

(2) Select the correct switch positions for I/O signature analysis and ensure that both LED 1 is ON and LED 2 is flashing.

(3) Signatures can now be checked on the following boards:

| | | | |
|---|---|---|---|
| (a) | A6A2 processor board | : | Tables 14.5 and 14.6 inclusive |
| (b) | A9A2 front panel memory board | : | Table 14.7 |
| (c) | A4 Main IF board | : | Table 14.8 Deleted |
| (d) | A6A1 Score board (If fitted) | : | Table 14.9 |
| (e) | A5 ISB board (If fitted) | : | Table 14.10 |
| (f) | A7 1st LO/Synthesizer board (Mk4 LSI only) | : | Table 14.11 |
| (g) | 2nd LO/BFO Synthesizer board | : | Table 14.12 |

Use of Signature Tables

70. The tables should be checked against the faulty unit working from top to bottom and from left to right. e.g. in Table 14.5 all signatures on U2 should be tested, then all on U4 etc. The first entrys in all tables are the 0 V and +V signatures. These not only check supplies to IC's but also serve as an indication of the nature of other faults. If a faulty signature is found, consult the board circuit diagram and ensure that this is the first occurrence of the fault in the circuit to establish which is the driving logic.

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P82120 Iss. 6)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | CCAF | | 12 | | | 5 | 5 | 5 | |
| A4 | AP18 | | 11 | | | 4 | 4 | 4 | |
| A5 | 10C8 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P82121 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 33P4 | | 12 | | | 5 | 5 | 5 | |
| A4 | C899 | | 11 | | | 4 | 4 | 4 | |
| A5 | 8FU3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P82122 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | A9CP | | 12 | | | 5 | 5 | 5 | |
| A4 | 7F6A | | 11 | | | 4 | 4 | 4 | |
| A5 | F6H5 | | 10 | | | 3 | 3 | 3 | |
| A6 | H76C | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P82123 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0HA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | 21U6 | | 12 | | | 5 | 5 | 5 | |
| A4 | 78U9 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P11 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5UAU | | 9 | | | 2 | 2 | 2 | |
| A7 | 713A | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P83045 Iss. 5)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | 0HUA | | 13 | | | 6 | 6 | 6 | |
| A3 | 6UP3 | | 12 | | | 5 | 5 | 5 | |
| A4 | CP60 | | 11 | | | 4 | 4 | 4 | |
| A5 | 0242 | | 10 | | | 3 | 3 | 3 | |
| A6 | 9CC4 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P83046 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | UOCA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | OHUA | | 13 | | | 6 | 6 | 6 | |
| A3 | P7AC | | 12 | | | 5 | 5 | 5 | |
| A4 | 7FAP | | 11 | | | 4 | 4 | 4 | |
| A5 | UHH3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 6425 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P83047 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | CCAF | | 12 | | | 5 | 5 | 5 | |
| A4 | AP18 | | 11 | | | 4 | 4 | 4 | |
| A5 | 10C8 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P83048 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 33P4 | | 12 | | | 5 | 5 | 5 | |
| A4 | C899 | | 11 | | | 4 | 4 | 4 | |
| A5 | 8FU3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84164 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | P35P | | 14 | | | 7 | 7 | 7 | |
| A2 | 659C | | 13 | | | 6 | 6 | 6 | |
| A3 | 4FH0 | | 12 | | | 5 | 5 | 5 | |
| A4 | HC97 | | 11 | | | 4 | 4 | 4 | |
| A5 | 3HA9 | | 10 | | | 3 | 3 | 3 | |
| A6 | H5P9 | | 9 | | | 2 | 2 | 2 | |
| A7 | 7334 | | 8 | | | 1 | 1 | 1 | |
| A8 | F1U7 | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84165 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | U8UC | | 13 | | | 6 | 6 | 6 | |
| A3 | P38C | | 12 | | | 5 | 5 | 5 | |
| A4 | C940 | | 11 | | | 4 | 4 | 4 | |
| A5 | 1H1F | | 10 | | | 3 | 3 | 3 | |
| A6 | 0FA2 | | 9 | | | 2 | 2 | 2 | |
| A7 | AA7U | | 8 | | | 1 | 1 | 1 | |
| A8 | C85A | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84166 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | 0HUA | | 13 | | | 6 | 6 | 6 | |
| A3 | 6UP3 | | 12 | | | 5 | 5 | 5 | |
| A4 | 3628 | | 11 | | | 4 | 4 | 4 | |
| A5 | F6H5 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5U23 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84167 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 87PP | | 13 | | | 6 | 6 | 6 | |
| A3 | 8P8F | | 12 | | | 5 | 5 | 5 | |
| A4 | 2A3A | | 11 | | | 4 | 4 | 4 | |
| A5 | 1UAC | | 10 | | | 3 | 3 | 3 | |
| A6 | H5P9 | | 9 | | | 2 | 2 | 2 | |
| A7 | 7334 | | 8 | | | 1 | 1 | 1 | |
| A8 | F1U7 | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84168 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | P35P | | 14 | | | 7 | 7 | 7 | |
| A2 | PHH3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 8997 | | 12 | | | 5 | 5 | 5 | |
| A4 | U6PC | | 11 | | | 4 | 4 | 4 | |
| A5 | C470 | | 10 | | | 3 | 3 | 3 | |
| A6 | 2H86 | | 9 | | | 2 | 2 | 2 | |
| A7 | 8C5C | | 8 | | | 1 | 1 | 1 | |
| A8 | 997P | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84170 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | 85C2 | | 13 | | | 6 | 6 | 6 | |
| A3 | F2F5 | | 12 | | | 5 | 5 | 5 | |
| A4 | 9779 | | 11 | | | 4 | 4 | 4 | |
| A5 | 76UU | | 10 | | | 3 | 3 | 3 | |
| A6 | PU09 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84178 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 33P4 | | 12 | | | 5 | 5 | 5 | |
| A4 | C899 | | 11 | | | 4 | 4 | 4 | |
| A5 | 8FU3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84179 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | 21U6 | | 12 | | | 5 | 5 | 5 | |
| A4 | 78U9 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P11 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5UAU | | 9 | | | 2 | 2 | 2 | |
| A7 | 713A | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84615 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | CCAF | | 12 | | | 5 | 5 | 5 | |
| A4 | AP18 | | 11 | | | 4 | 4 | 4 | |
| A5 | 10C8 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84616 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 33P4 | | 12 | | | 5 | 5 | 5 | |
| A4 | C899 | | 11 | | | 4 | 4 | 4 | |
| A5 | 8FU3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84617 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | A9CP | | 12 | | | 5 | 5 | 5 | |
| A4 | 7F6A | | 11 | | | 4 | 4 | 4 | |
| A5 | F6H5 | | 10 | | | 3 | 3 | 3 | |
| A6 | H76C | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84618 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | 21U6 | | 12 | | | 5 | 5 | 5 | |
| A4 | 78U9 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P11 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5UAU | | 9 | | | 2 | 2 | 2 | |
| A7 | 713A | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84619 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | 21U6 | | 12 | | | 5 | 5 | 5 | |
| A4 | 78U9 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P11 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5UAU | | 9 | | | 2 | 2 | 2 | |
| A7 | 713A | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES P84662 Issue 1

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | 85C2 | | 13 | | | 6 | 6 | 6 | |
| A3 | F2F5 | | 12 | | | 5 | 5 | 5 | |
| A4 | 9779 | | 11 | | | 4 | 4 | 4 | |
| A5 | 76UU | | 10 | | | 3 | 3 | 3 | |
| A6 | PU09 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84626 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P7U3 | | 15 | | | 8 | 8 | 8 | |
| A1 | A3CF | | 14 | | | 7 | 7 | 7 | |
| A2 | U62A | | 13 | | | 6 | 6 | 6 | |
| A3 | HC1C | | 12 | | | 5 | 5 | 5 | |
| A4 | OPFU | | 11 | | | 4 | 4 | 4 | |
| A5 | 3PCA | | 10 | | | 3 | 3 | 3 | |
| A6 | SHA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84627 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P7U3 | | 15 | | | 8 | 8 | 8 | |
| A1 | A3CF | | 14 | | | 7 | 7 | 7 | |
| A2 | U62A | | 13 | | | 6 | 6 | 6 | |
| A3 | 5353 | | 12 | | | 5 | 5 | 5 | |
| A4 | 78U9 | | 11 | | | 4 | 4 | 4 | |
| A5 | F4HC | | 10 | | | 3 | 3 | 3 | |
| A6 | H565 | | 9 | | | 2 | 2 | 2 | |
| A7 | 713A | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84628 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6UCC | | 15 | | | 8 | 8 | 8 | |
| A1 | C64A | | 14 | | | 7 | 7 | 7 | |
| A2 | A6U5 | | 13 | | | 6 | 6 | 6 | |
| A3 | 4863 | | 12 | | | 5 | 5 | 5 | |
| A4 | 0P84 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P9H | | 10 | | | 3 | 3 | 3 | |
| A6 | 5U23 | | 9 | | | 2 | 2 | 2 | |
| A7 | UC7F | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P84629 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6UCC | | 15 | | | 8 | 8 | 8 | |
| A1 | C64A | | 14 | | | 7 | 7 | 7 | |
| A2 | A6U5 | | 13 | | | 6 | 6 | 6 | |
| A3 | F02C | | 12 | | | 5 | 5 | 5 | |
| A4 | PCFA | | 11 | | | 4 | 4 | 4 | |
| A5 | UHFF | | 10 | | | 3 | 3 | 3 | |
| A6 | PF72 | | 9 | | | 2 | 2 | 2 | |
| A7 | UC7F | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85060 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P7U3 | | 15 | | | 8 | 8 | 8 | |
| A1 | A3CF | | 14 | | | 7 | 7 | 7 | |
| A2 | U62A | | 13 | | | 6 | 6 | 6 | |
| A3 | HC1C | | 12 | | | 5 | 5 | 5 | |
| A4 | OPFU | | 11 | | | 4 | 4 | 4 | |
| A5 | 3PCA | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85061 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P7U3 | | 15 | | | 8 | 8 | 8 | |
| A1 | A3CF | | 14 | | | 7 | 7 | 7 | |
| A2 | U62A | | 13 | | | 6 | 6 | 6 | |
| A3 | 5353 | | 12 | | | 5 | 5 | 5 | |
| A4 | 78U9 | | 11 | | | 4 | 4 | 4 | |
| A5 | F4HC | | 10 | | | 3 | 3 | 3 | |
| A6 | H565 | | 9 | | | 2 | 2 | 2 | |
| A7 | 713A | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85062 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6UCC | | 15 | | | 8 | 8 | 8 | |
| A1 | C64A | | 14 | | | 7 | 7 | 7 | |
| A2 | A6U5 | | 13 | | | 6 | 6 | 6 | |
| A3 | 4863 | | 12 | | | 5 | 5 | 5 | |
| A4 | 0P84 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P9H | | 10 | | | 3 | 3 | 3 | |
| A6 | 5U23 | | 9 | | | 2 | 2 | 2 | |
| A7 | UC7F | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85063 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6UCC | | 15 | | | 8 | 8 | 8 | |
| A1 | C64A | | 14 | | | 7 | 7 | 7 | |
| A2 | A6U5 | | 13 | | | 6 | 6 | 6 | |
| A3 | F02C | | 12 | | | 5 | 5 | 5 | |
| A4 | PCFA | | 11 | | | 4 | 4 | 4 | |
| A5 | UHFF | | 10 | | | 3 | 3 | 3 | |
| A6 | PF72 | | 9 | | | 2 | 2 | 2 | |
| A7 | UC7F | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP. | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85068 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | A9CP | | 12 | | | 5 | 5 | 5 | |
| A4 | 7F6A | | 11 | | | 4 | 4 | 4 | |
| A5 | F6H5 | | 10 | | | 3 | 3 | 3 | |
| A6 | H76C | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | S641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85069 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | A9CP | | 12 | | | 5 | 5 | 5 | |
| A4 | 7F6A | | 11 | | | 4 | 4 | 4 | |
| A5 | F6H5 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5U23 | | 9 | | | 2 | 2 | 2 | |
| A7 | 71C6 | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85412 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | UOCA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | P35P | | 14 | | | 7 | 7 | 7 | |
| A2 | PHH3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 01HU | | 12 | | | 5 | 5 | 5 | |
| A4 | 5A19 | | 11 | | | 4 | 4 | 4 | |
| A5 | P63C | | 10 | | | 3 | 3 | 3 | |
| A6 | 7UFH | | 9 | | | 2 | 2 | 2 | |
| A7 | 71C6 | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359S | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85413 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | 85C2 | | 13 | | | 6 | 6 | 6 | |
| A3 | F2F5 | | 12 | | | 5 | 5 | 5 | |
| A4 | 9779 | | 11 | | | 4 | 4 | 4 | |
| A5 | 76UU | | 10 | | | 3 | 3 | 3 | |
| A6 | PU09 | | 9 | | | 2 | 2 | 2 | |
| A7 | 71C6 | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85414 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P7U3 | | 15 | | | 8 | 8 | 8 | |
| A1 | A3CF | | 14 | | | 7 | 7 | 7 | |
| A2 | U62A | | 13 | | | 6 | 6 | 6 | |
| A3 | HC1C | | 12 | | | 5 | 5 | 5 | |
| A4 | OPFU | | 11 | | | 4 | 4 | 4 | |
| A5 | C6U2 | | 10 | | | 3 | 3 | 3 | |
| A6 | 2U04 | | 9 | | | 2 | 2 | 2 | |
| A7 | 8C5C | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC 997P | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85415 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P7U3 | | 15 | | | 8 | 8 | 8 | |
| A1 | A3CF | | 14 | | | 7 | 7 | 7 | |
| A2 | U62A | | 13 | | | 6 | 6 | 6 | |
| A3 | 5353 | | 12 | | | 5 | 5 | 5 | |
| A4 | 78UA | | 11 | | | 4 | 4 | 4 | |
| A5 | 4F93 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85416 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6UCC | | 15 | | | 8 | 8 | 8 | |
| A1 | C64A | | 14 | | | 7 | 7 | 7 | |
| A2 | A6U5 | | 13 | | | 6 | 6 | 6 | |
| A3 | 4863 | | 12 | | | 5 | 5 | 5 | |
| A4 | 0P84 | | 11 | | | 4 | 4 | 4 | |
| A5 | F6H5 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85417 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6UCC | | 15 | | | 8 | 8 | 8 | |
| A1 | C64A | | 14 | | | 7 | 7 | 7 | |
| A2 | A6U5 | | 13 | | | 6 | 6 | 6 | |
| A3 | F02C | | 12 | | | 5 | 5 | 5 | |
| A4 | PCFA | | 11 | | | 4 | 4 | 4 | |
| A5 | 7584 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85421 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 33P4 | | 12 | | | 5 | 5 | 5 | |
| A4 | C899 | | 11 | | | 4 | 4 | 4 | |
| A5 | 8FU3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85670 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | P35P | | 14 | | | 7 | 7 | 7 | |
| A2 | 659C | | 13 | | | 6 | 6 | 6 | |
| A3 | 4FH0 | | 12 | | | 5 | 5 | 5 | |
| A4 | HC97 | | 11 | | | 4 | 4 | 4 | |
| A5 | 3HA9 | | 10 | | | 3 | 3 | 3 | |
| A6 | H5P9 | | 9 | | | 2 | 2 | 2 | |
| A7 | 7334 | | 8 | | | 1 | 1 | 1 | |
| A8 | F1U7 | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85671 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | 0HUA | | 13 | | | 6 | 6 | 6 | |
| A3 | P7AC | | 12 | | | 5 | 5 | 5 | |
| A4 | 7FAP | | 11 | | | 4 | 4 | 4 | |
| A5 | UHH3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 6423 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85672 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | CCAF | | 12 | | | 5 | 5 | 5 | |
| A4 | AP18 | | 11 | | | 4 | 4 | 4 | |
| A5 | 10C8 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | |
|---|---|
| D0 | |
| D1 | |
| D2 | Due to unpredictable propagation delays |
| D3 | in the microprocessors, reliable |
| D4 | signatures are not possible on the databus |
| D5 | |
| D6 | |
| D7 | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85675 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 87PP | | 13 | | | 6 | 6 | 6 | |
| A3 | 06F4 | | 12 | | | 5 | 5 | 5 | |
| A4 | 81H3 | | 11 | | | 4 | 4 | 4 | |
| A5 | 18FP | | 10 | | | 3 | 3 | 3 | |
| A6 | 8138 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85676 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 87PP | | 13 | | | 6 | 6 | 6 | |
| A3 | 06F4 | | 12 | | | 5 | 5 | 5 | |
| A4 | 81H3 | | 11 | | | 4 | 4 | 4 | |
| A5 | 18FP | | 10 | | | 3 | 3 | 3 | |
| A6 | 8138 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85674 Iss. 2)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | P35P | | 14 | | | 7 | 7 | 7 | |
| A2 | PHH3 | | 13 | | | 6 | 6 | 6 | |
| A3 | B997 | | 12 | | | 5 | 5 | 5 | |
| A4 | U6PC | | 11 | | | 4 | 4 | 4 | |
| A5 | C470 | | 10 | | | 3 | 3 | 3 | |
| A6 | 2H86 | | 9 | | | 2 | 2 | 2 | |
| A7 | 0313 | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85677 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | UOCA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | A9CP | | 12 | | | 5 | 5 | 5 | |
| A4 | U422 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4800 | | 10 | | | 3 | 3 | 3 | |
| A6 | H1U6 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85678 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | CCAF | | 12 | | | 5 | 5 | 5 | |
| A4 | AP18 | | 11 | | | 4 | 4 | 4 | |
| A5 | 98U0 | | 10 | | | 3 | 3 | 3 | |
| A6 | 0106 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85679 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6UCC | | 15 | | | 8 | 8 | 8 | |
| A1 | 3P02 | | 14 | | | 7 | 7 | 7 | |
| A2 | 6P81 | | 13 | | | 6 | 6 | 6 | |
| A3 | C92P | | 12 | | | 5 | 5 | 5 | |
| A4 | 3253 | | 11 | | | 4 | 4 | 4 | |
| A5 | 0639 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85868 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 33P4 | | 12 | | | 5 | 5 | 5 | |
| A4 | C899 | | 11 | | | 4 | 4 | 4 | |
| A5 | 8FU3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85869 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | UOCA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 33PH | | 12 | | | 5 | 5 | 5 | |
| A4 | C899 | | 11 | | | 4 | 4 | 4 | |
| A5 | 8FU3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | - | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85870 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | 0HUA | | 13 | | | 6 | 6 | 6 | |
| A3 | 6UP3 | | 12 | | | 5 | 5 | 5 | |
| A4 | 3628 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P9H | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85871 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | CCAF | | 12 | | | 5 | 5 | 5 | |
| A4 | 2560 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4F1U | | 10 | | | 3 | 3 | 3 | |
| A6 | SHA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85872 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 87PP | | 13 | | | 6 | 6 | 6 | |
| A3 | 06F4 | | 12 | | | 5 | 5 | 5 | |
| A4 | 81H3 | | 11 | | | 4 | 4 | 4 | |
| A5 | 18FP | | 10 | | | 3 | 3 | 3 | |
| A6 | 8138 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85874 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | P35P | | 14 | | | 7 | 7 | 7 | |
| A2 | 659C | | 13 | | | 6 | 6 | 6 | |
| A3 | F498 | | 12 | | | 5 | 5 | 5 | |
| A4 | 3A6A | | 11 | | | 4 | 4 | 4 | |
| A5 | 8650 | | 10 | | | 3 | 3 | 3 | |
| A6 | 1UA6 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85875 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | 21U6 | | 12 | | | 5 | 5 | 5 | |
| A4 | 78U9 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P11 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5UAU | | 9 | | | 2 | 2 | 2 | |
| A7 | 713A | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85876 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000 | 38 | | | | | | | |
| XTLY | C04F | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | 0HUA | | 13 | | | 6 | 6 | 6 | |
| A3 | P7AC | | 12 | | | 5 | 5 | 5 | |
| A4 | U4P6 | | 11 | | | 4 | 4 | 4 | |
| A5 | 73F2 | | 10 | | | 3 | 3 | 3 | |
| A6 | SHA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85877 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000 | 38 | | | | | | | |
| XTLY | C04F | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | U42A | | 14 | | | 7 | 7 | 7 | |
| A2 | 85C2 | | 13 | | | 6 | 6 | 6 | |
| A3 | F2F5 | | 12 | | | 5 | 5 | 5 | |
| A4 | 9779 | | 11 | | | 4 | 4 | 4 | |
| A5 | 76UU | | 10 | | | 3 | 3 | 3 | |
| A6 | PU09 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P85879 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 33P4 | | 12 | | | 5 | 5 | 5 | |
| A4 | C899 | | 11 | | | 4 | 4 | 4 | |
| A5 | 8FU3 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P86500 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | 21UP | | 12 | | | 5 | 5 | 5 | |
| A4 | 78U9 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P11 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5UAU | | 9 | | | 2 | 2 | 2 | |
| A7 | 713A | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (86501 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | A9CP | | 12 | | | 5 | 5 | 5 | |
| A4 | U422 | | 11 | | | 4 | 4 | 4 | |
| A5 | 4800 | | 10 | | | 3 | 3 | 3 | |
| A6 | 59CP | | 9 | | | 2 | 2 | 2 | |
| A7 | 772C | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | |
|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (86503 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 28OF | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | OUA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | A9CP | | 12 | | | 5 | 5 | 5 | |
| A4 | 7F6A | | 11 | | | 4 | 4 | 4 | |
| A5 | 4P9H | | 10 | | | 3 | 3 | 3 | |
| A6 | HSP9 | | 9 | | | 2 | 2 | 2 | |
| A7 | UC7F | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A541 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P86504 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | P35P | | 14 | | | 7 | 7 | 7 | |
| A2 | PHH3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 8997 | | 12 | | | 5 | 5 | 5 | |
| A4 | U6PC | | 11 | | | 4 | 4 | 4 | |
| A5 | 3F38 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | 71C6 | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P86508 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | P571 | | 15 | | | 8 | 8 | 8 | |
| A1 | 6C16 | | 14 | | | 7 | 7 | 7 | |
| A2 | 70C3 | | 13 | | | 6 | 6 | 6 | |
| A3 | 33P4 | | 12 | | | 5 | 5 | 5 | |
| A4 | C899 | | 11 | | | 4 | 4 | 4 | |
| A5 | 04CC | | 10 | | | 3 | 3 | 3 | |
| A6 | 9H4H | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | CHH2 | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus | | | | | | | |
| D3 | | | | | | | | | |
| D4 | | | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

## TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (86880 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6UCC | | 15 | | | 8 | 8 | 8 | |
| A1 | C64A | | 14 | | | 7 | 7 | 7 | |
| A2 | A6U5 | | 13 | | | 6 | 6 | 6 | |
| A3 | F02C | | 12 | | | 5 | 5 | 5 | |
| A4 | PCFA | | 11 | | | 4 | 4 | 4 | |
| A5 | 7584 | | 10 | | | 3 | 3 | 3 | |
| A6 | 5HA1 | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |

| | | |
|---|---|---|
| D0<br>D1<br>D2<br>D3<br>D4<br>D5<br>D6<br>D7 | | Due to unpredictable propagation delays in the microprocessors, reliable signatures are not possible on the databus |

TABLE 14.5 A6A2 PROCESSOR BOARD (ROM) SIGNATURES (P86885 Iss. 1)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U2 | U4 | U5 | U7 | U8 | U9 | U11 | U15 |
| 0 V | 0000 | 24,40 | 20 | 7 | 8 | 12 | 12 | 12 | 8 |
| + V | C04F | 3,4 | 1,7,40 | 14 | 16 | 21,24 | 21,24 | 24 | 16 |
| ROMC 0 | 01HU | 17 | 35 | | | | | | |
| ROMC 1 | CC23 | 18 | 36 | | | | | | |
| ROMC 2 | A093 | 19 | 37 | | | | | | |
| ROMC 3 | P15U | 20 | 38 | | | | | | |
| ROMC 4 | U0CA | 21 | 39 | | | | | | |
| WRITE | H09F | 2 | 3 | | | | | | |
| /INT REQ | C04F | 23 | 4 | | | | | | |
| /RESET | C04F | 37 | | | | | | | |
| XTLX | 0000(F) | 38 | | | | | | | |
| XTLY | C04F(F) | 39 | | | | | | | |
| /PRI IN | C04F | | 5 | | | | | | |
| RAM WRITE | C04H | | 6 | | | | | 21 | 7 |
| CPU READ | 9840 | | 34 | 13 | | | | | |
| /CPU READ | 280F | | | 12 | 1 | | | | |
| A0 | 6H39 | | 15 | | | 8 | 8 | 8 | |
| A1 | 7F62 | | 14 | | | 7 | 7 | 7 | |
| A2 | 0UA6 | | 13 | | | 6 | 6 | 6 | |
| A3 | A9CP | | 12 | | | 5 | 5 | 5 | |
| A4 | 7F6A | | 11 | | | 4 | 4 | 4 | |
| A5 | F6H5 | | 10 | | | 3 | 3 | 3 | |
| A6 | H76C | | 9 | | | 2 | 2 | 2 | |
| A7 | U9UP | | 8 | | | 1 | 1 | 1 | |
| A8 | PCHC | | 25 | | | 23 | 23 | 23 | |
| A9 | A641 | | 26 | | | 22 | 22 | 22 | |
| A10 | 359A | | 27 | | | 19 | 19 | 19 | |
| A11 | 6HPP | | 28 | | | 18 | 18 | | |
| A12 | PUPP | | 29 | | 2,14 | | | | |
| A13 | 6686 | | 30 | | 3,13 | | | | |
| A14 | 0000 | | 31 | | | | | | |
| A15 | 0000 | | 32 | | | | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U7 | U8 | U9 | U11 | U13 | U15 | U2 | U4 |
| 0 V | 0000 | 8 | 12 | 12 | 12 | 8 | 8 | 24 | 20 |
| + V | C04F | 16 | 21,24 | 21,24 | 24 | 16 | 16 | 3,4 | 1,40 |
| U7A/Y0 | 88F1 | 4 | 20 | | | | | | |
| Y1 | 1081 | 5 | | 20 | | | | | |
| Y2 | C04F | 6 | | | 20 | | | | |
| Y3 | C04F | 7 | | | | 1 | | | |
| U7B/Y2 | 3PA7 | 10 | | | 18 | | | | |
| Y3 | 5821 | 9 | | | | | 9,10 | | |
| D0 | | | | | | | | | |
| D1 | | | | | | | | | |
| D2 | | Due to unpredictable propagation delays | | | | | | | |
| D3 | | in the microprocessors, reliable | | | | | | | |
| D4 | | signatures are not possible on the databus | | | | | | | |
| D5 | | | | | | | | | |
| D6 | | | | | | | | | |
| D7 | | | | | | | | | |

TABLE 14.6 A6A2 PROCESSOR BOARD (I/O) SIGNATURES

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | |
|---|---|---|---|---|---|---|---|
| | | U2 | U1 | U3 | U5 | U6 | U10 |
| 0 V | 0000 | | | | | | |
| +V | 8714 | | | | | | |
| ROMC 0 | F787 | 17 | 4 | 12 | 11 | | |
| ROMC 1 | 50C8 | 18 | 13 | | | | |
| ROMC 2 | U7A5 | 19 | | 3 | | | |
| ROMC 3 | 56FP | 20 | 1 | | | | |
| ROMC 4 | 56P6 | 21 | 2 | | | | |
| - | P2P1 | | 12 | 2 | | | |
| I/O | 6SU5 | | 3,9 | 1,6 | 5 | | |
| WRITE | 8714 | | 11 | | 1 | | |
| - | 4093 | | 10 | | 10 | | |
| /WSTB | P2P1 | | 8 | | | | |
| /OE | P2P1 | | | 9,11 | 6 | 1 | |
| /WRITE | 0000(F) | | | 5 | 2 | | |
| CP | P2P1 | | | 4 | | 11 | |
| D0 | HU68 | 15 | | | | 3 | 2 |
| 1 | P44F | 12 | | | | 4 | 3 |
| 2 | 1AP6 | 9 | | | | 7 | 4 |
| 3 | 53HH | 6 | | | | 8 | 5 |
| 4 | 4PPH | 35 | | | | 13 | 6 |
| 5 | 64UC | 32 | | | | 14 | 7 |
| 6 | 286P | 29 | | | | 17 | 8 |
| 7 | 1169 | 26 | | | | 18 | 9 |
| IOCO | F198 | | | | | 2 | |
| 1 | 3048 | | | | | 5 | |
| 2 | C2OF | | | | | 6 | |
| 3 | 79OU | | | | | 9 | |
| 4 | H25U | | | | | 12 | |
| 5 | P735 | | | | | 15 | |
| 6 | F3PO | | | | | 16 | |
| 7 | UNSTABLE with score) | | | | | | |
| | PC3C without score) | | | 8 | | 19 | |
| - | 3H89 | | | 10 | 9 | | |
| $\overline{G}$ | CA9H | | | | 8 | | 19 |
| DIR | 65U5 | | | 13 | | | 1 |

TABLE 14.6 A6A2 PROCESSOR BOARD (I/O) SIGNATURES (cont'd)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | |
|---|---|---|---|
| | | U10 | U2 |
| 10D 0 | 00A8 | 18 | |
| 1 | UPCP | 17 | |
| 2 | 8U00 | 16 | |
| 3 | U96P | 15 | |
| 4 | CF92 | 14 | |
| 5 | 9U40 | 13 | |
| 6 | 27P8 | 12 | |
| 7 | C1FC | 11 | |
| I/O PORT 0 00 | 76F4 | | 16 |
| 01 | 15U7 | | 11 |
| 02 | 3F6F | | 10 |
| 03 | 31A2 | | 5 |
| 04 | H3OP | | 36 |
| 05 | 47FC | | 31 |
| 06 | A1H9 | | 30 |
| 07 | HFU5 | | 25 |
| I/O PORT 1 00 | CC60 | | 14 |
| 01 | 23AF | | 13 |
| 12 | A9FA | | 8 |
| 13 | 6AC9 | | 7 |
| 14 | 0000 / H212 | | 34 |
| 15 | 3723 / 3723 | | 33 |
| 16 | 0000 / FPA7 | | 28 |
| 17 | 0000 / U73H | | 27 |

NOTE: WITH / WITHOUT SCORE

TABLE 14.7 A9A2 FRONT PANEL MEMORY BOARD (I/O) SIGNATURES

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U8 | U10 | U7 | U6 | U5 | U3 | U16 | U17 |
| 0 V | 0000 | 12 | 7,8 | 7 | 7 | 7 | 7 | 8 | 8 |
| +V | 8714 | 24 | 16 | 14 | 14 | 14 | 14 | 16 | 16 |
| IOC 0 | F198 | 2 | 11 | | | | | | |
| IOC 1 | 3048 | 3 | 10 | | | | | | |
| IOC 2 | C20F | 21 | 9 | 1 | | | | | |
| IOC 3 | 790U | 22 | | | | | | | |
| IOC 4 | H25U | | | | 2 | | | | |
| IOC 5 | P735 | | | 12,13 | 1,13 | | 13 | | |
| IOC 6 | F3P0 | | | | | 6 | 12 | | |
| /IO READ | 8714 | | 3 | 2,5,6 | | | | | |
| /WSTB | P2P1 | | | 8 | | | 11,2 | | |
| - | 6021 | | 6 | 11 | | | | | |
| - | 0000 | | | 3 | 12 | | | | |
| - | 8714 | | | | 11 | | | 1 | 1 |
| - | 0000 | | | 4 | | 5 | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | U8 | U10 | U7 | U6 | U5 | U3 | U16 | U17 |
| IOC 0 | F188 | 2 | 11 | | | | | | |
| 1 | 3048 | 3 | 10 | | | | | | |
| 2 | C20F | 21 | 9 | 1 | | | | | |
| 3 | 790U | 22 | | | | | | | |
| 4 | H25U | | | | 2 | | | | |
| 5 | P735 | | | 12,13 | 1,13 | | 13 | | |
| 6 | F3P0 | | | | | 6 | 12 | | |
| $\overline{\text{IOREAD}}$ | 8714 | | 3 | 2,5,6 | | | | | |
| $\overline{\text{WSTB}}$ | P2P1 | | | 8 | | | 11,2 | | |
| - | 6021 | | 6 | 11 | | | | | |
| - | 0000 | | | 3 | 12 | | | | |
| - | 8714 | | | | 11 | | | 1 | 1 |
| - | 0000 | | | 4 | | 5 | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | U19 | U20 | U13 | U14 | U15 | U16 | U17 | U18 | U3 |
| IOD 0 | 00A8 | 4 | | 13 | | | | 9,13 | 9 | |
| 1 | UPCP | 14 | | 12 | | | | 7,11 | 7 | |
| 2 | 8U00 | 7 | | 11 | | 11 | | 5 | 5 | |
| 3 | U96P | 13 | | 10 | | 13 | | 3 | 3 | |
| 4 | CF92 | | 4 | | 13 | 9 | 9 | | 13 | |
| 5 | 9U40 | | 14 | | 12 | 7 | 7 | | 11 | |
| 6 | 27P8 | | 13 | | 11 | 3 | 3,13 | | | |
| 7 | CIFC | | 7 | | 10 | 5 | 5,11 | | | |
| CK TO U19/U20 | 6021 | 5 | 5 | | | | | | | 1 |

TABLE 14.7 A9A2 FRONT PANEL MEMORY BOARD (I/O) SIGNATURES (Cont'd)

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | U19 | U20 | U24 | U25 | U26 | U27 | U12 | U13 | U14 |
| DB0 | 0C40 | 2 | | 11 | 11 | 11 | 11 | 4 | 19 | 19 |
| 1 | 405F | 1 | | 12 | 12 | 12 | 12 | 12 | 20 | 20 |
| 2 | PC7C | 10 | | 13 | 13 | 13 | 13 | 13 | 21 | 21 |
| 3 | 2FU7 | 11 | | 14 | 14 | 14 | 14 | 3 | 3 | 3 |
| 4 | 1F99 | | 2 | 9 | | | | | 4 | 4 |
| 5 | C7A2 | | 1 | | 9 | | | | 5 | 5 |
| 6 | AF80 | | 11 | | | 9 | | | 6 | 6 |
| 7 | 0F3U | | 10 | | | | 9 | | | |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | |
|---|---|---|---|---|---|---|---|
| | | U8 | U24 | U25 | U26 | U27 | |
| STROBE TO BFO LATCH | 0U83 | 18 | 7 | 7 | 7 | 7 | |
| 10 Hz | 30C4 | | 6 | | | | |
| 20 Hz | 8405 | | 5 | | | | |
| 40 Hz | 6PC7 | | 4 | | | | |
| 80 Hz | 5306 | | 3 | | | | |
| 100 Hz | 30C4 | | | 6 | | | |
| 200 Hz | 8405 | | | 5 | | | |
| 400 Hz | 6PC7 | | | 4 | | | |
| 800 Hz | A2FU | | | 3 | | | |
| 1 kHz | 30C4 | | | | 6 | | |
| 2 kHz | 8405 | | | | 5 | | |
| 4 kHz | 6PC7 | | | | 4 | | |
| 8 kHz | A2FU | | | | 3 | | |
| 10 kHz | 30C4 | | | | | 6 | |
| 20 kHz | 8405 | | | | | 5 | |
| 40 kHz | 6PC7 | | | | | 4 | |

TABLE 14.8 MAIN IF/AF BOARD (I/O) SIGNATURES

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | U3 | U5 | U2 | U4 | U13 | U15 | U21 | U23 | U25 |
| D80 | 0C40 | 3 | | | | | | | | |
| 1 | 405F | 6 | | | | | | | | |
| 2 | PC7C | 10 | | | | | | | | |
| 3 | 2FU7 | 14 | | | | | | | | |
| 4 | IF99 | | 3 | | | | | | | |
| 5 | C7A2 | | 6 | | | | | | | |
| 6 | AF80 | | 10 | | | | | | | |
| 6 | 0F3U | | 14 | | | | | | | |
| D80 | PPUC | 4 | | 14 | | 14 | | 11 | 13 | |
| 1 | F595 | 5 | | 13 | | 13 | | 10 | 7 | |
| 2 | U074 | 11 | | 7 | | 7 | | 9 | 4 | |
| 3 | 0H74 | 13 | | 4 | | 4 | | 8 | | 6 |
| 4 | AUFU | | 4 | | 14 | | 14 | 7 | | 5 |
| 5 | 6887 | | 5 | | 13 | | 13 | 6 | | 4 |
| 6 | 0965 | | 11 | | 7 | | 7 | 5 | | 3 |
| 7 | 4745 | | 13 | | 4 | | 4 | 4 | | 2 |

TABLE 14.9 A6A1 REMOTE CONTROL SCORE INTERFACE (I/O) SIGNATURES

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | U19 | U23 | U25 | U20 | U14 | U21 | U24 |
| PB0 | HU68 | 21 | 11 | | | | | |
| 1 | P44F | 22 | 12 | | | | | |
| 2 | 1AP6 | 27 | 13 | | | | | |
| 3 | 53HH | 28 | 14 | | | | | |
| 4 | 4PPH | 33 | 7 | | | | | |
| 5 | 64UC | 34 | 6 | | | | | |
| 6 | 286P | 39 | 5 | | | | | |
| 7 | 1169 | | 4 | 3 | | | | |
| ROMC 0 | F787 | 17 | | | 6 | | | |
| 1 | 50C8 | 16 | | | 10 | | | |
| 2 | U7A5 | 15 | | | 7 | | | |
| 3 | 56FP | 14 | | | 2 | | | |
| 4 | 56P6 | 13 | | | 15 | | | |
| WRITE | 8714(F) | 7 | | | | | | |
| /INT REQ | 8714(H) | 9 | | | | | | |
| /PRI | 8714(H) | 6 | | | | | | |
| /ICB | 8714(H) | 10 | | | | 7 | | |
| IOREAD | 8714 | | | | | | 12 | |
| IOC3 | 790U | | | | | | 5 | |
| IOC7 | UNSTABLE | | | | | | 6 | |
| I/O PORT 0 00 | 76F4 | | | | | | 1 | |
| 01 | 15U7 | | | | | | | 15 |
| 02 | 3F6F | | | | | | | 14 |
| 03 | 31A2 | | | | | | | 13 |
| 04 | H3OP | | | | | | | 4 |
| 05 | 47FC | | | | | | | 5 |
| 06 | A1H9 | | | | | | | 6 |
| 07 | HFU5 | | | | | | | 7 |

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | | |
|---|---|---|---|---|---|---|
| | | U22 | U12 | U14 | U8 | U7 |
| I/O PORT 1 10 | CC60 | 4 | | | | |
| 11 | 23AF | 8 | | | | |
| 12 | A9FA | | 5 | | | |
| 13 | 6AC9 | 6 | | | | |
| 14 | 0000 | | | 2 | | |
| 15 | UNSTABLE | | | 15 | | |
| 16 | 0000 | | | | 5 | |
| 17 | 0000 | | | | | 3 |

TABLE 14.10 A5 ISB AF/IF MODULE (I/O) SIGNATURES

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | |
|---|---|---|---|
| | | U8 | U7 |
| D80 | PPUC | 14 | |
| 1 | F595 | 13 | |
| 2 | U074 | 7 | |
| 3 | 0H74 | 4 | |
| 4 | AUFU | | 14 |
| 5 | 6887 | | 13 |
| 6 | 0965 | | 7 |
| 7 | 4745 | | 4 |

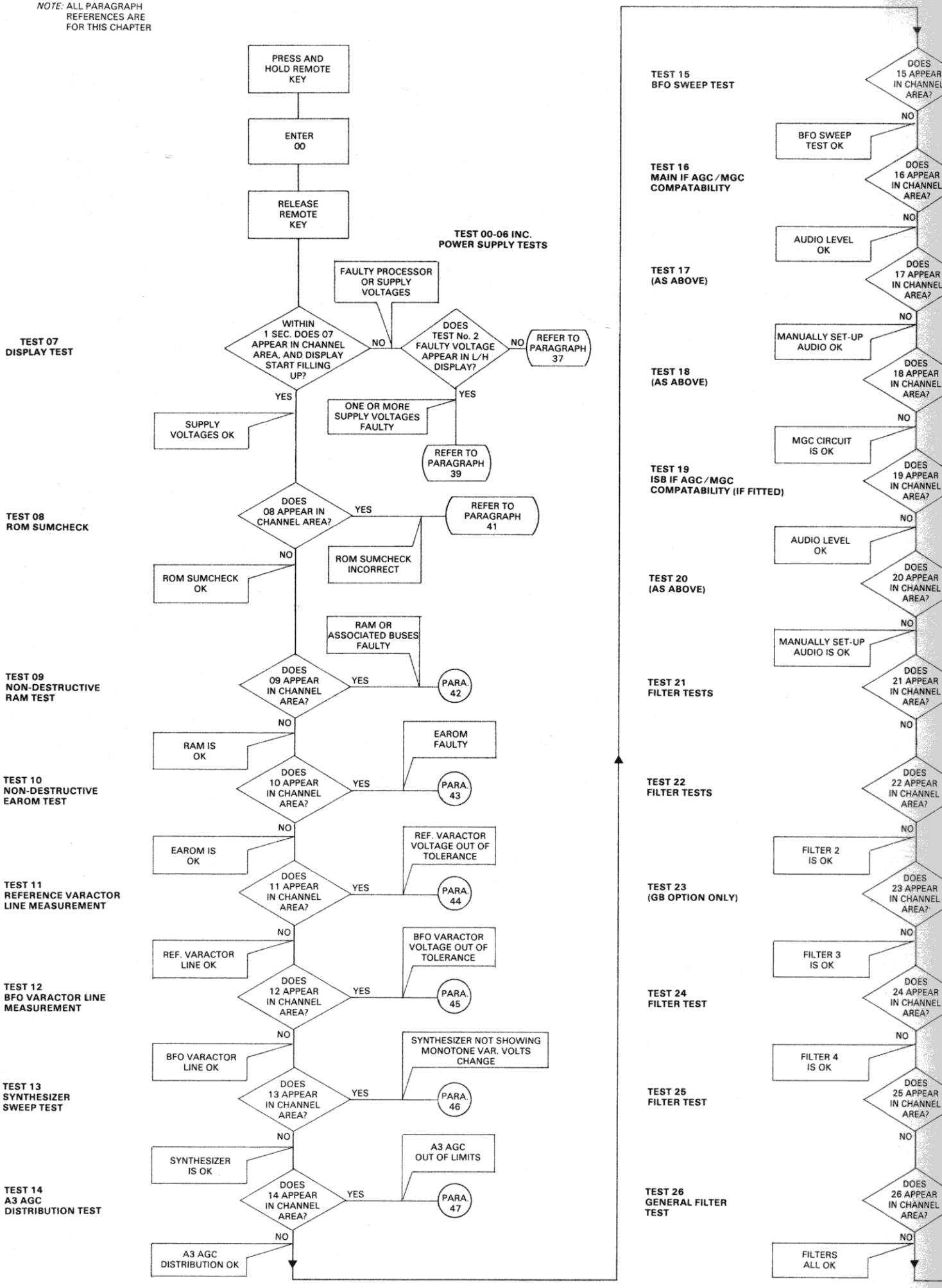
TABLE 14.11 A7 FIRST LO SYNTHESIZER (MK4) (I/O) SIGNATURES

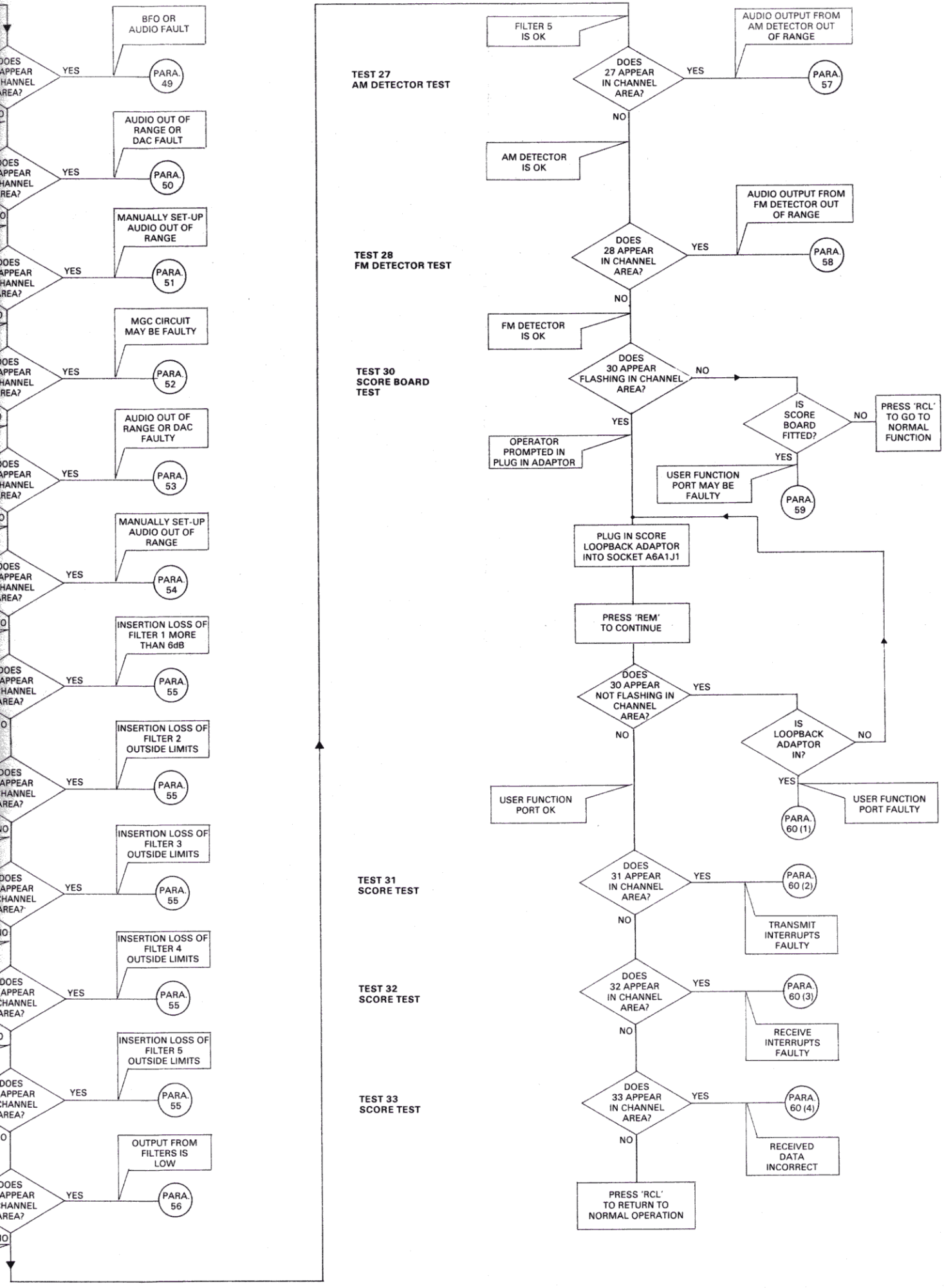
| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) |
|---|---|---|
| | | U9 |
| 0 V | 0000 | |
| +V | 8714 | |
| DB0 | 0C40 | 22 |
| 1 | 4U5F | 21 |
| 2 | PC7C | 20 |
| 3 | 2FU7 | 19 |
| 4 | 1F99 | 18 |

TABLE 14.12 A8 SECOND LO/BFO SYNTHESIZER (I/O) SIGNATURES

| SIGNAL IDENT | SIGNATURE | CIRCUIT REFERENCE (DEVICE AND PIN NUMBER) | | | |
|---|---|---|---|---|---|
| | | U18 | U17 | U16 | U15 |
| 10 Hz | 30C4 | 3 | | | |
| 20 Hz | 8405 | 4 | | | |
| 40 Hz | 6PC7 | 5 | | | |
| 80 Hz | 5306 | 6 | | | |
| 100 Hz | 30C4 | | 3 | | |
| 200 Hz | 8405 | | 4 | | |
| 400 Hz | 6PC7 | | 5 | | |
| 800 Hz | A2FU | | 6 | | |
| 1 kHz | 30C4 | | | 3 | |
| 2 kHz | 8405 | | | 4 | |
| 4 | 6PC7 | | | 5 | |
| 8 | A2FU | | | 6 | |
| 10 | 30C4 | | | | 3 |
| 20 | 8405 | | | | 4 |
| 40 | 6PC7 | | | | 5 |

*NOTE:* ALL PARAGRAPH REFERENCES ARE FOR THIS CHAPTER






**BITE FLOWCHART**

FIG. 14.4

# CHAPTER 15

# INTERCONNECTIONS

## CONTENTS


| Para | | Page |
|---|---|---|
| 1 | INTRODUCTION<br>COMPONENTS LIST | 15-1 |


## ILLUSTRATIONS


| Fig. | |
|---|---|
| 15-1 | RA 1792 : Interconnections Diagram (Type 85830) |

# CHAPTER 15

# INTERCONNECTIONS

## INTRODUCTION

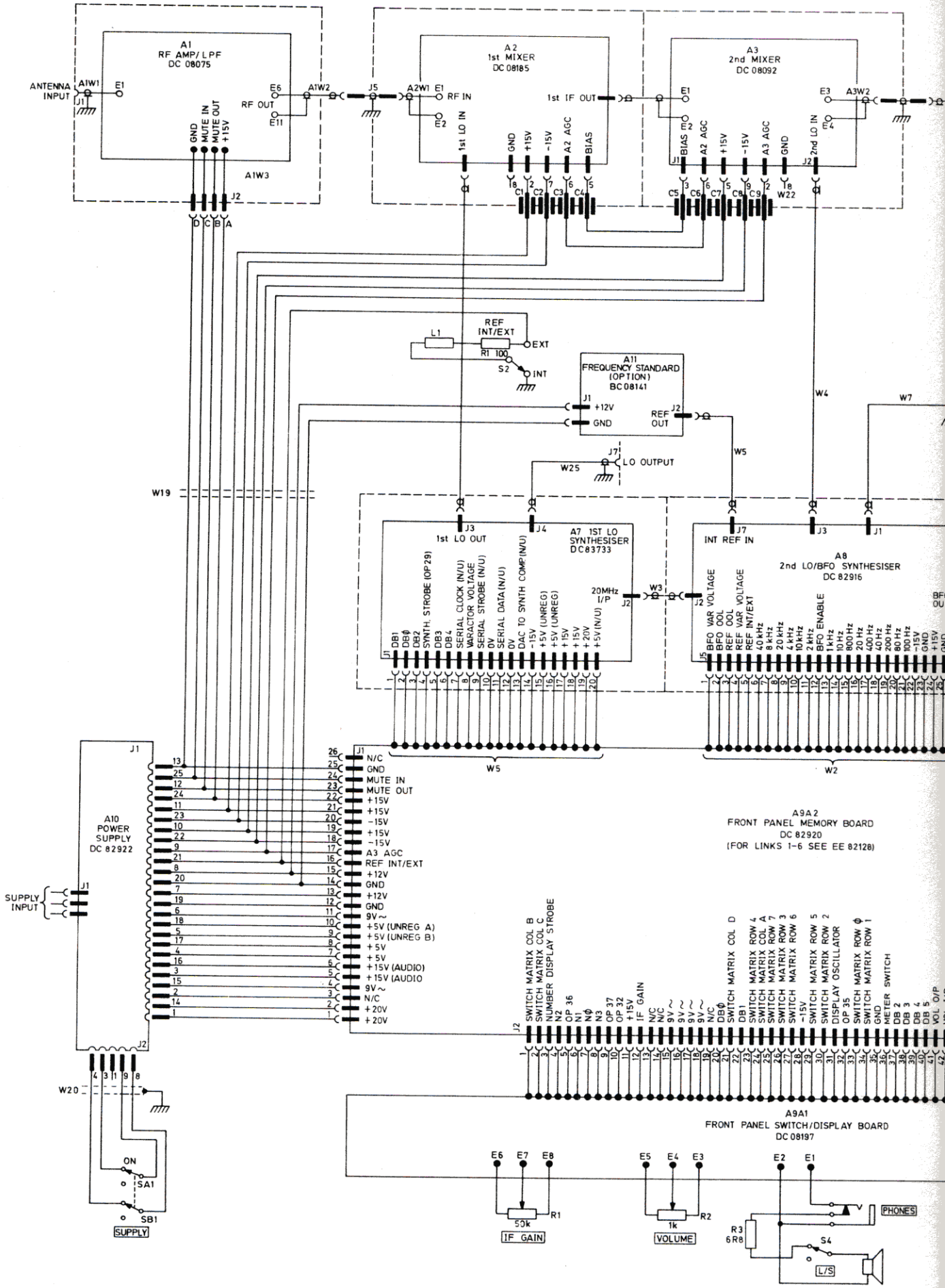
1. Fig. 15-1 shows interconnections for the RA 1792 receiver.

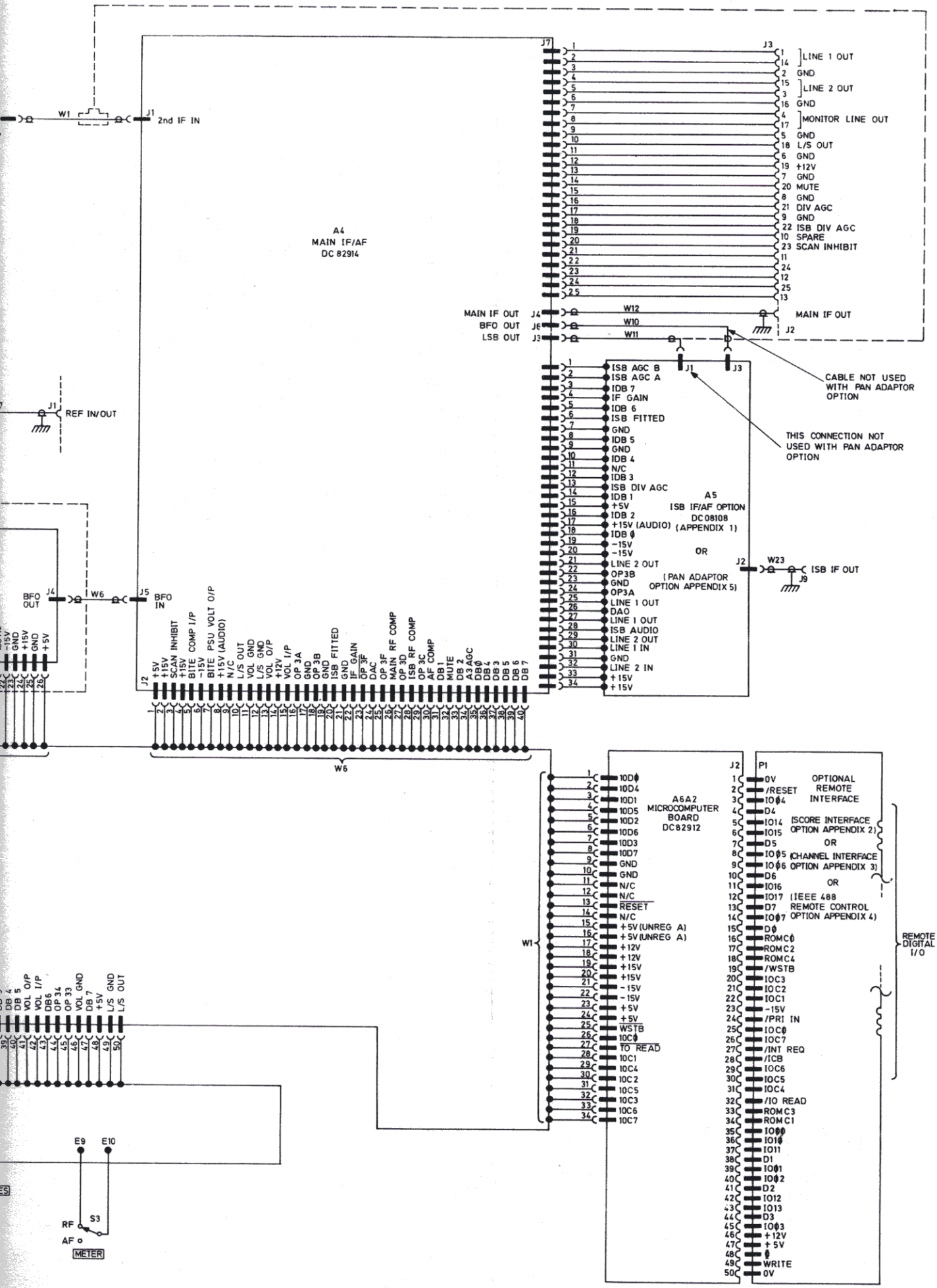
## MAINS CHASSIS (ST 82910, ST 82128)

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | Ω | | W | | |
| R1 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| **Capacitors** | | | | | |
| C1-C9 | 1n | Feed Through | 500 | 20 | 939678 |
| **Inductors** | µH | | | | |
| L1 | 100 | Choke | | | 919471 |
| **Connectors** | | | | | |
| J1 | | Jack Suhner Bulkhead | | | 919499 |
| J2 | | Jack Suhner Bulkhead | | | 919499 |
| J3 | | Socket 25-way | | | 941994 |
| J5 | | Plug Bulkhead | | | 938654 |
| J6 | | Plug Bulkhead | | | 938654 |
| **Miscellaneous** | | | | | |
| S2 | | Switch Slide DPDT | | | 938666 |

## FRONT PANEL SUB ASSEMBLY (ST 82921)

| | | | | | |
|---|---|---|---|---|---|
| **Resistors** | Ω | | W | | |
| R1 | 50k | Potentiometer IF Gain | | | B08243 |
| R2 | 1k | Potentiometer Volume Control | | | 943858 |
| **Miscellaneous** | | | | | |
| LS1 | | Loudspeaker | | | 938669 |
| S1 | | Switch Rocker | | | 938535 |
| S3 | | Switch Rocker | | | 938535 |
| S4 | | Switch Rocker | | | 938535 |


A1
RF AMP/LPF
DC 08075
ANTENNA INPUT
A1W1
E1
J1
E6
RF OUT
E11
A1W2
GND
MUTE IN
MUTE OUT
+15V
A1W3
J2
D C B A
J5
A2W1
E1
RF IN
E2
A2
1st MIXER
DC 08185
1st IF OUT
1st LO IN
GND
+15V
-15V
A2 AGC
BIAS
A3
2nd MIXER
DC 08092
E1
E2
BIAS
A2 AGC
+15V
-15V
A3 AGC
GND
2nd LO IN
E4
E3
A3W2
J1
J2
C1 C2 C3 C4
C5 C6 C7 C8 C9
W22
L1
REF INT/EXT
EXT
R1 100
S2
INT
A11
FREQUENCY STANDARD
(OPTION)
BC 08141
+12V
GND
REF OUT
W4
W7
W5
J7
LO OUTPUT
W25
W19
J3
1st LO OUT
J4
A7 1ST LO
SYNTHESISER
DC 83733
20MHz I/P
W3
J7
INT REF IN
A8
2nd LO/BFO SYNTHESISER
DC 82916
DB1
DBØ
DB2
SYNTH. STROBE (OP 29)
DB3
DB4
SERIAL CLOCK (N/U)
VARACTOR VOLTAGE
SERIAL STROBE (N/U)
0V
SERIAL DATA (N/U)
0V
DAC TO SYNTH COMP (N/U)
-15V
+5V (UNREG)
+5V (UNREG)
+15V
+15V
+20V
+5V (N/U)
BFO VAR VOLTAGE
BFO OOL
REF OOL
REF VAR VOLTAGE
REF INT/EXT
40 kHz
8 kHz
20 kHz
4 kHz
10 kHz
2 kHz
BFO ENABLE
1 kHz
10 Hz
800 Hz
20 Hz
400 Hz
40 Hz
200 Hz
80 Hz
100 Hz
-15V
GND
+15V
W5
W2
A10
POWER
SUPPLY
DC 82922
SUPPLY INPUT
N/C
GND
MUTE IN
MUTE OUT
+15V
+15V
-15V
+15V
-15V
A3 AGC
REF INT/EXT
+12V
GND
+12V
GND
9V~
+5V (UNREG A)
+5V (UNREG B)
+5V
+5V
+15V (AUDIO)
+15V (AUDIO)
9V~
N/C
+20V
+20V
A9A2
FRONT PANEL MEMORY BOARD
DC 82920
(FOR LINKS 1-6 SEE EE 82128)
SWITCH MATRIX COL B
SWITCH MATRIX COL C
NUMBER DISPLAY STROBE
N2
OP 36
N1
NØ
N3
OP 37
OP 32
+15V
IF GAIN
N/C
N/C
9V~
9V~
9V~
9V~
N/C
DBØ
SWITCH MATRIX COL D
DB1
SWITCH MATRIX ROW 4
SWITCH MATRIX COL A
SWITCH MATRIX ROW 7
SWITCH MATRIX ROW 3
SWITCH MATRIX ROW 6
SWITCH
-15V
SWITCH MATRIX ROW 5
SWITCH MATRIX ROW 2
DISPLAY OSCILLATOR
OP 35
SWITCH MATRIX ROW Ø
SWITCH MATRIX ROW 1
GND
METER SWITCH
DB 2
DB 3
DB 4
DB 5
VOL O/P
A9A1
FRONT PANEL SWITCH/DISPLAY BOARD
DC 08197
W20
ON
SA1
SB1
SUPPLY
E6 E7 E8
50k
R1
IF GAIN
E5 E4 E3
1k
R2
VOLUME
E2 E1
PHONES
R3
6R8
S4
L/S




# RA 1792 (Type 85830)
# Interconnection Diagram

Fig.15·1

# APPENDIX 1

# ISB IF/AF MODULE A5

## CONTENTS


| Para | | Page |
|---|---|---|
| 1 | INTRODUCTION | App. 1-1 |
| 3 | CIRCUIT DESCRIPTION | App. 1-1 |
| 4 | AGC Controlled IF Amplifier | App. 1-1 |
| 5 | OPERATION OF AGC CIRCUITRY | App. 1-1 |
| 6 | PRODUCT DETECTOR | App. 1-2 |
| 7 | AUDIO AMPLIFIERS | App. 1-2 |
| | COMPONENTS LIST | |


## ILLUSTRATIONS


| Fig. No. | |
|---|---|
| App.1.1 | SIMIPLIFIED BLOCK DIAGRAM: ISB IF/AF MODULE A5 |
| App.1.2 | CIRCUIT: ISB IF/AF MODULE A5 |
| App.1.3 | COMPONENT LAYOUT: ISB IF/AF MODULE A5 |

# APPENDIX 1

## ISB IF/AF MODULE A5

### INTRODUCTION

1. The ISB IF/AF Module provides optional indendent sideband operation for the RA 1792 HF Receiver. The A5 module is substantially similar to the main ISB IF/AF Module A4 (chapter 5). A simplified block diagram of the ISB IF/AF module is given in Fig. 1 and the circuit diagram is given in Fig. 2, both at the end of this appendix.

2. This module contains a second IF amplifier, product detector and associated AF amplifiers, together with IF output and AGC circuits. Solid state switching circuits are also included for AGC time constants and AGC Dump.

### CIRCUIT DESCRIPTION

3. Selection of the position of LK1 on the Main IF/AF board allows filter FL1 (lower sideband) to be connected to the ISB IF/AF board, whilst leaving the other filters connected to the main circuitry. For modes other than ISB, only one filter is selected. When the ISB option is used, however, two filters are selected under software control, FL1 and FL2 (upper sideband).

#### AGC Controlled IF Amplifier

4. The source impedance of the signal from the selected filter is transformed from 5 k ohms to about 200 ohms by Q1 and the signal is then applied to an integrated circuit gain-controlled amplifier, U6. This device contains two amplifier sections which are connected in cascade to provide high gain and AGC range. The input signal is applied via C5 to pin 1, and the output from the first section, at pin 12, is applied via R19 and C13 to the input of the second section at pin 10. The output taken from pin 7 is applied via a bandpass filter to an emitter follower, Q3, and also to the IF output amplifier comprising Q2, Q4 and Q5, and from there to the rear panel IF OUT connector J9 at a level of 100 mV.

### OPERATION OF AGC CIRCUITRY

5. The signal from the AGC controlled IF amplifier (U6) is fed via Q3, which is connected as an emitter follower, to the AGC detector which comprises U2a, b and c. U2a and c provide an envelope of the audio signal available at TP7, whilst U2b provides thermal stability for U2c. The envelope is in the form of a DC voltage. The DC voltage following the audio envelope at TP4 passes into U3c, which detects the peak of the envelope. The peak voltage is then applied to the integrator, U10a, whose output falls with rising input peak values. The output voltage (available on TP8) is buffered by U3d and then leaves the ISB board via P1 pin 1, passing to J8 pin 1 on the main IF/AF board. There, the AGC voltage is applied to U17c, where the two AGC levels are summed by U17d. AGC 'hang' and 'dump' are as described in chapter 5.

PRODUCT DETECTOR

6. The lower-sideband IF signal enters the ISB board via J3, is amplified by Q7 and is passed to the product detector, U11. Audio is low-pass filtered and then buffered by Q8. The audio signal leaves the ISB board by P1 pin 28, to be connected to the Audio Crosspoint switch on the Main IF/AF board (see Chapter 5, para. 26).

AUDIO AMPLIFIERS

7. U12 contains two audio amplifiers which receive input via P1 pin 30 (Line 1 in) and pin 32 (Line 2 in) from the Audio Crosspoint switch on the Main IF/AF board (Chapter 5). The outputs from the two amplifiers, via T1 and T2, give balanced outputs or unbalanced outputs by connection of links LK1 and LK2.

## ISB IF/AF MODULE (ST 08108)

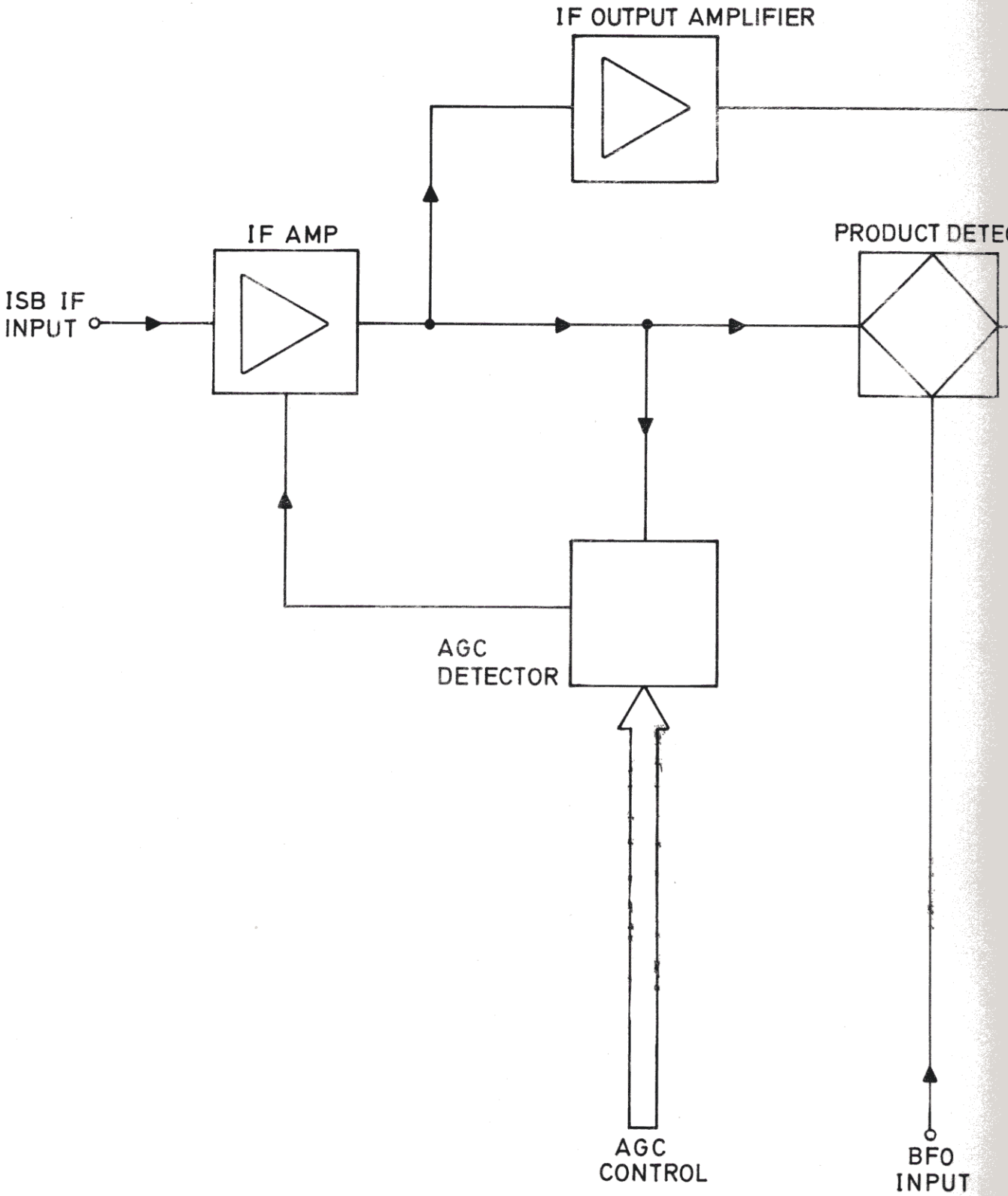
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R1 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R2 | 1.5k | Metal Oxide | ¼ | 2 | 911166 |
| R3 | 56k | Metal Oxide | ¼ | 2 | 913497 |
| R4 | 12k | Metal Oxide | ¼ | 2 | 917952 |
| R5 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R6 | 3.3k | Metal Oxide | ¼ | 2 | 910111 |
| R7 | 2.7k | Metal Oxide | ¼ | 2 | 916548 |
| R8 | 560 | Metal Oxide | ¼ | 2 | 917061 |
| R9 | 47k | Metal Oxide | ¼ | 2 | 913496 |
| R10 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R11 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R12 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R13 | 47k | Metal Oxide | ¼ | 2 | 913496 |
| R14 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R15 | 47k | Metal Oxide | ¼ | 2 | 913496 |
| R16 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R17 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R18 | 1.5k | Metal Oxide | ¼ | 2 | 911166 |
| R19 | 2k | Variable | | | 938440 |
| R20 | 220k | Metal Oxide | ¼ | 2 | 921771 |
| R21 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R22 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R23 | 50 | Metal Oxide | ¼ | 2 | 938441 |
| R24 | 680 | Metal Oxide | ¼ | 2 | 910113 |
| R25 | 2.2k | Metal Oxide | ¼ | 2 | 916546 |
| R26 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R27 | 4.7k | Metal Oxide | ¼ | 2 | 913490 |
| R28 | 47k | Metal Oxide | ¼ | 2 | 913496 |
| R29 | 33k | Metal Oxide | ¼ | 2 | 913495 |
| R30 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R31 | | Not Used | | | |
| R32 | | Not Used | | | |
| R33 | 47 | Metal Oxide | ¼ | 2 | 917063 |
| R34 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R35 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R36 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R37 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R38 | 1.5k | Metal Oxide | ¼ | 2 | 911166 |
| R39 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R40 | 15k | Metal Oxide | ¼ | 2 | 920645 |

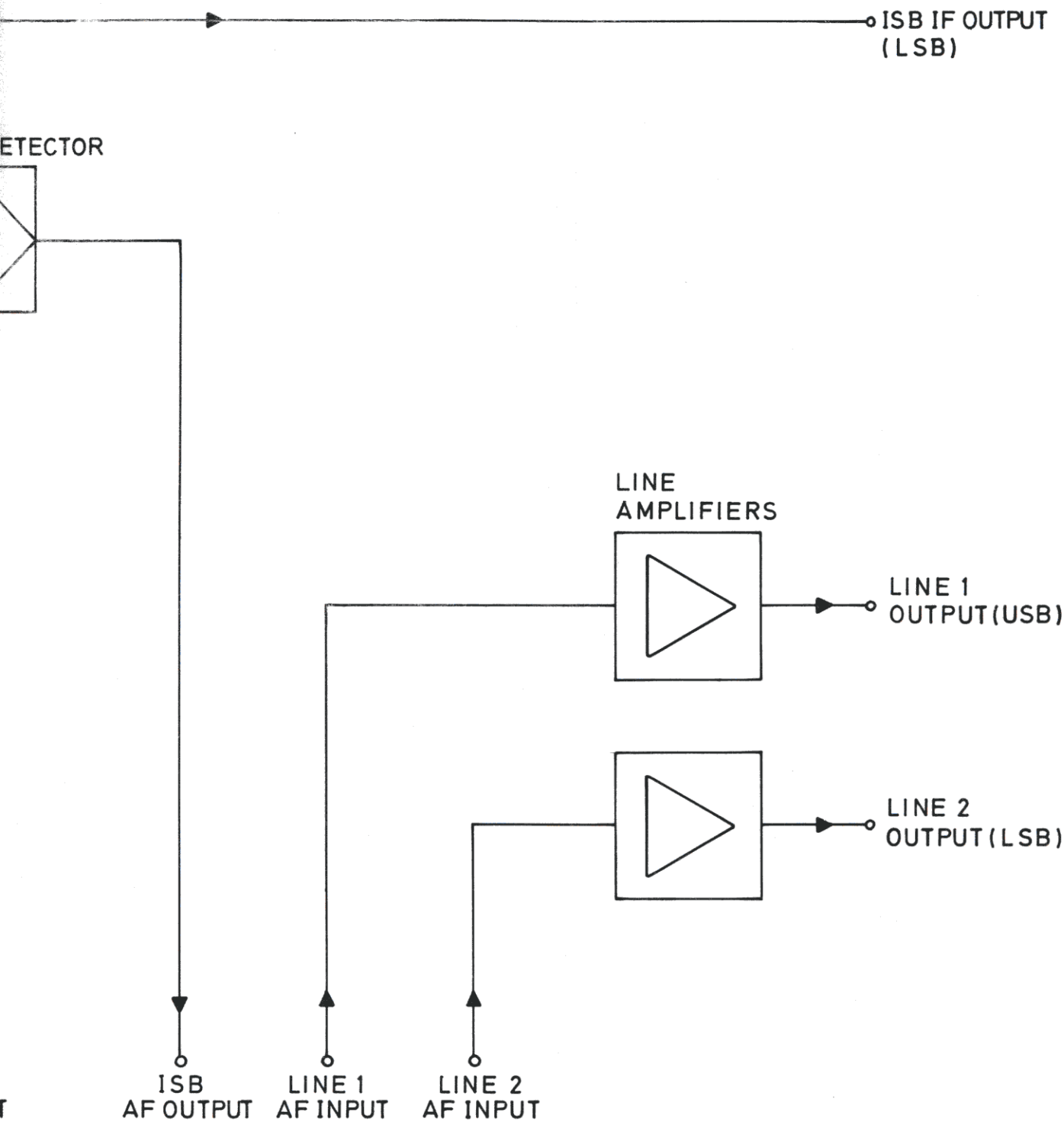
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R41 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R42 | 1.2k | Metal Oxide | ¼ | 2 | 911179 |
| R43 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R44 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R45 | 15k | Metal Oxide | ¼ | 2 | 920645 |
| R46 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R47 | 390 | Metal Oxide | ¼ | 2 | 916331 |
| R48 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R49 | 18k | Metal Oxide | ¼ | 2 | 900994 |
| R50 | 39 | Metal Oxide | ¼ | 2 | 917062 |
| R51 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R52 | 3.3k | Metal Oxide | ¼ | 2 | 910111 |
| R53 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R54 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R55 | 33k | Metal Oxide | ¼ | 2 | 913495 |
| R56 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R57 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R58 | 22k | Metal Oxide | ¼ | 2 | 913493 |
| R59 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R60 | 33 | Metal Oxide | ¼ | 2 | 917060 |
| R61 | 390 | Metal Oxide | ¼ | 2 | 916331 |
| R62 | | Not Used | | | |
| R63 | 10k | Metal Oxide | ¼ | 2 | 914042 |
| R64 | 470 | Metal Oxide | ¼ | 2 | 920758 |
| R65 | 3.3k | Metal Oxide | ¼ | 2 | 910111 |
| R66 | 3.3k | Metal Oxide | ¼ | 2 | 910111 |
| R67 | 3.3k | Metal Oxide | ¼ | 2 | 910111 |
| R68 | 1.2k | Metal Oxide | ¼ | 2 | 911179 |
| R69 | 3.3k | Metal Oxide | ¼ | 2 | 910111 |
| R70 | 27k | Metal Oxide | ¼ | 2 | 913494 |
| R71 | 27k | Metal Oxide | ¼ | 2 | 913494 |
| R72 | 4.7k | Metal Oxide | ¼ | 2 | 913490 |
| R73 | 4.7k | Metal Oxide | ¼ | 2 | 913490 |
| R74 | 39k | Metal Oxide | ¼ | 2 | 900993 |
| R75 | 68k | Metal Oxide | ¼ | 2 | 916478 |
| R76 | 100k | Metal Oxide | ¼ | 2 | 915190 |
| R77 | 100k | Metal Oxide | ¼ | 2 | 915190 |
| R78 | 4.7k | Metal Oxide | ¼ | 2 | 913490 |
| R79 | 8.2k | Metal Oxide | ¼ | 2 | 918202 |
| R80 | | Not Used | | | |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | W | | |
| R81 | 2.2k | Metal Oxide | ¼ | 2 | 916546 |
| R82 | 33 | Metal Oxide | ¼ | 2 | 917060 |
| R83 | 22 | Metal Oxide | ¼ | 2 | 920743 |
| R84 | 33 | Metal Oxide | ¼ | 2 | 917060 |
| R85 | 10 | Metal Oxide | ¼ | 2 | 920736 |
| R86 | 270k | Metal Oxide | ¼ | 2 | 923598 |
| R87 | 1k | Metal Oxide | ¼ | 2 | 913489 |
| R88 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| R89 | 100 | Metal Oxide | ¼ | 2 | 910388 |
| Capacitors | | | V | | |
| C1 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C2 | 0.001 | Ceramic | 50 | 20 | 938408 |
| C3 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C4 | 100 | Electrolytic | 25 | -10 +50 | 935140 |
| C5 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C6 | 0.022 | Ceramic | 50 | 20 | 930219 |
| C7 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C8 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C9 | 15 | Tantalum | 20 | 20 | 938034 |
| C10 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C11 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C12 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C13 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C14 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C15 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C16 | 0.0015 | Mica | 500 | 2 | 943146 |
| C17 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C18 | 82p | Mica | 350 | 2 | 902232 |
| C19 | 0.0015 | Mica | 500 | 2 | 943146 |
| C20 | 15 | Tantalum | 20 | 20 | 938034 |
| C21 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C22 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C23 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C24 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C25 | 0.01 | Ceramic | 50 | 20 | 938053 |
| C26 | 15 | Tantalum | 20 | 20 | 938034 |
| C27 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C28 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C29 | | Not Used | | | |
| C30 | 0.1 | Ceramic | 50 | 20 | 938406 |

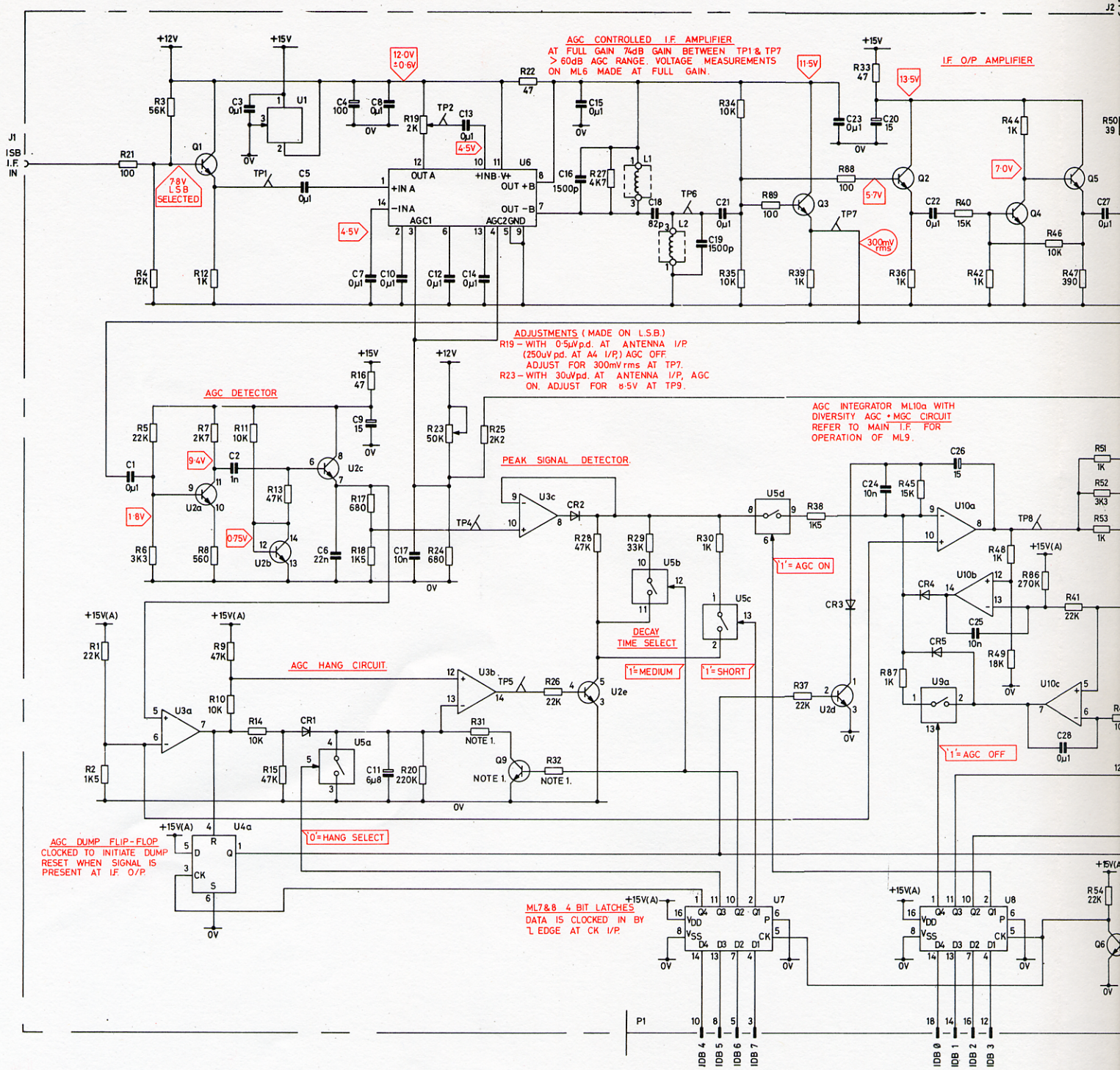
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Capacitors** | | | V | | |
| C31 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C32 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C33 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C34 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C35 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C36 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C37 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C38 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C39 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C40 | 220 | Electrolytic | 16 | -10 +50 | 938436 |
| C41 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C42 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C43 | 6.8 | Tantalum | 35 | 20 | 938030 |
| C44 | 0.0047 | Ceramic | 500 | 5 | 938437 |
| C45 | 0.1 | Ceramic | 50 | 20 | 938406 |
| C46 | 0.0022 | Ceramic | 500 | 5 | 938438 |
| C47 | 220 | Electrolytic | 16 | 5 | 938436 |
| C48 | 68 | Tantalum | 15 | 20 | 938036 |
| C49 | 68 | Tantalum | 15 | 20 | 938036 |
| C50 | 100 | Electrolytic | 25 | -10 +50 | 921546 |
| C51 | 6.8 | Tantalum | 50 | 20 | 943427 |
| C52 | 470 | Electrolytic | 25 | -10 +100 | 938439 |
| C53 | 15 | Tantalum | 20 | 20 | 938034 |
| C54 | 0.1 | Ceramic | 50 | 20 | 938406 |
| **Diodes** | | | | | |
| CR1 | | 1N916 | | | 913480 |
| CR2 | | 1N916 | | | 913480 |
| CR3 | | 1N916 | | | 913480 |
| CR4 | | 1N916 | | | 913480 |
| CR5 | | 1N916 | | | 913480 |
| CR6 | | 1N916 | | | 913480 |
| **Transistors** | | | | | |
| Q1 | | 2N5089 | | | 938417 |
| Q2 | | 2N5089 | | | 938417 |
| Q3 | | BC109 | | | 923234 |
| Q4 | | 2N5089 | | | 938417 |
| Q5 | | 2N5089 | | | 938417 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Transistors** | | | | | |
| Q6 | | 2N2369 | | | 906842 |
| Q7 | | 2N5089 | | | 938417 |
| Q8 | | 2N5089 | | | 938417 |
| **Integrated Circuits** | | | | | |
| U1 | | Voltage Regulator 78L12 | | | 938455 |
| U2 | | Transistor Array CA 3046 | | | 922907 |
| U3 | | Quad Op. Amp. LM324N | | | 925944 |
| U4 | | Dual 'D'-type flip-flop 4013 | | | 933644 |
| U5 | | Quad Bilateral Switch 4066 | | | 930148 |
| U6 | | IF Amp. 757 | | | 921201 |
| U7 | | Quad Latch 4042 | | | 938443 |
| U8 | | Quad Latch 4042 | | | 938443 |
| U9 | | Quad Bilateral Switch 4066 | | | 930148 |
| U10 | | Quad Op. Amp. LM324N | | | 925944 |
| U11 | | Balanced Modulator/Demodulator 1496 | | | 938427 |
| U12 | | Dual 2 W Audio Amplifier 377 | | | 928536 |
| U13 | | Voltage Regulator +12 V 7812 | | | 938445 |
| **Transformers** | | | | | |
| T1 | | Transformer Assy. | | | AT81401 |
| T2 | | Transformer Assy. | | | AT81401 |
| **Inductors** | | | | | |
| L1 | | Coil RF Variable | | | AT81400 |
| L2 | | Coil RF Variable | | | AT81400 |
| **Connectors** | | | | | |
| J1 | | Plug, RF 50 ohms | | | 938429 |
| J2 | | Plug, RF 50 ohms | | | 938429 |
| J3 | | Plug, RF 50 ohms | | | 938429 |
| **Miscellaneous** | | | | | |
| | | Cable assembly | | | B08226 |
| | | Comprising: | | | |
| | | Connector, Plug, PCB 34-way | | | 938571 |
| | | Socket, 34-way | | | 934213 |
| | | Clamp, Strain Relief | | | 934214 |
| | | Cable, PVC, 34-way | | | 927430 |


IF OUTPUT AMPLIFIER
IF AMP
PRODUCT DETE
ISB IF
INPUT
AGC
DETECTOR
AGC
CONTROL
BFO
INPUT

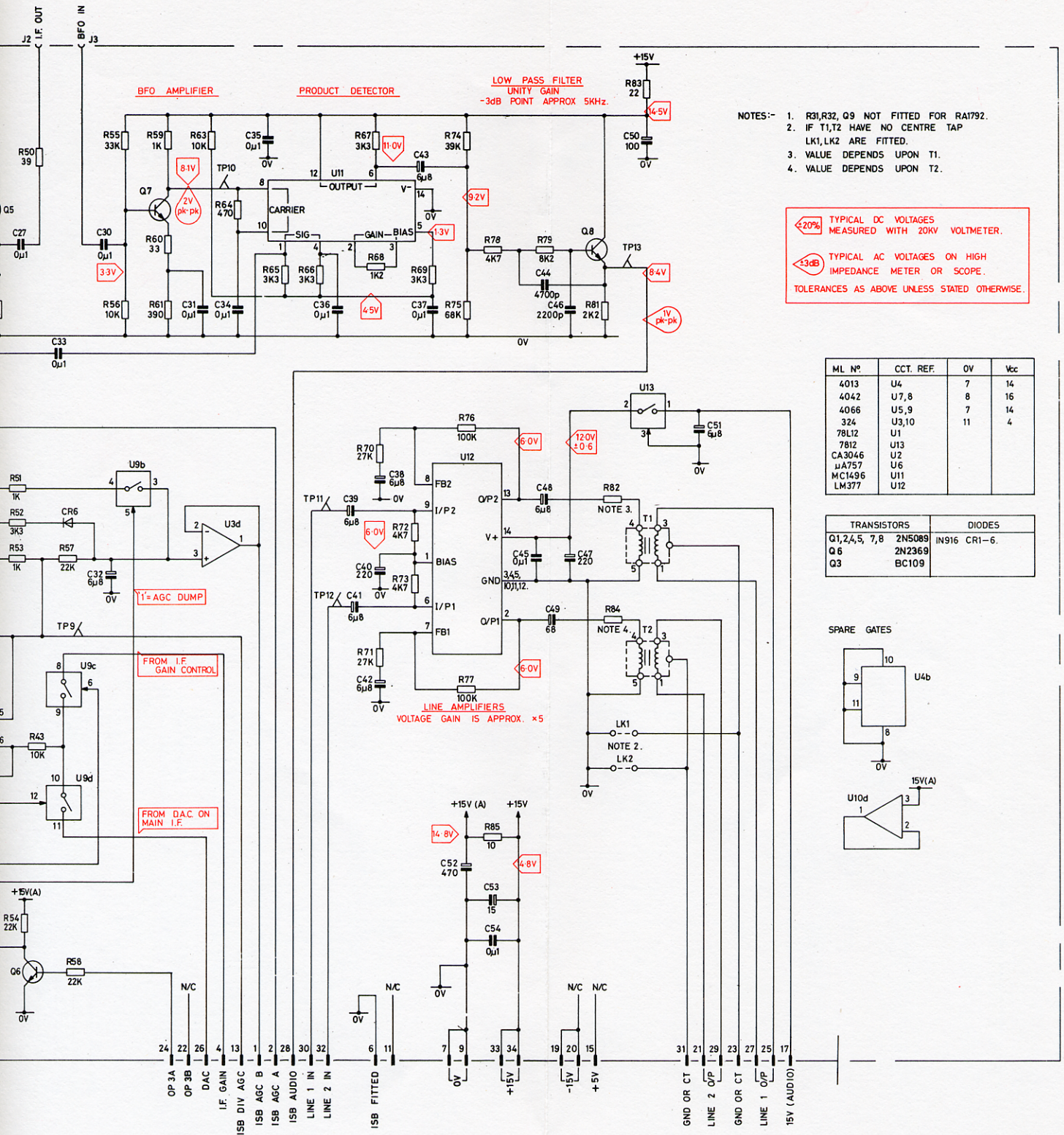



Simplified Block Diagram:
ISB I/F Module A5 Fig. App. 1.1




RACAL

| TH3416 | DC 08108/1 | TH3416 | DC 08108/2 |
|---|---|---|---|
| 5 | 7 | 5 | 7 |



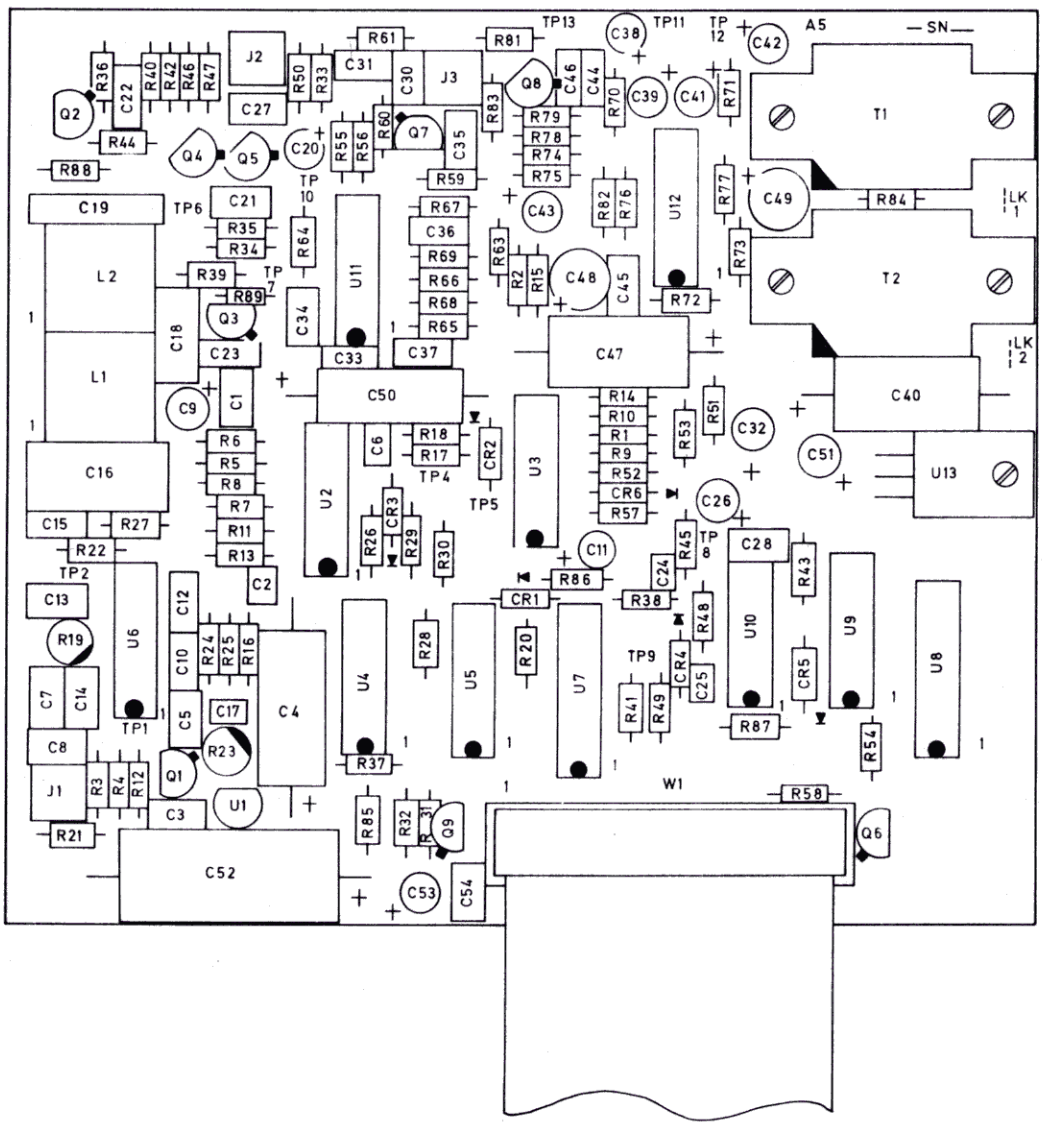

| ML Nº. | CCT. REF. | 0V | Vcc |
|---|---|---|---|
| 4013 | U4 | 7 | 14 |
| 4042 | U7,8 | 8 | 16 |
| 4066 | U5,9 | 7 | 14 |
| 324 | U3,10 | 11 | 4 |
| 78L12 | U1 | | |
| 7812 | U13 | | |
| CA3046 | U2 | | |
| µA757 | U6 | | |
| MC1496 | U11 | | |
| LM377 | U12 | | |

| TRANSISTORS | | DIODES |
|---|---|---|
| Q1,2,4,5, 7,8 | 2N5089 | IN916 CR1–6. |
| Q6 | 2N2369 | |
| Q3 | BC109 | |

SPARE GATES




**Circuit: ISB IF/AF Module A5** **Fig App.1.2**






Layout : ISB IF/AF Board A5

Fig. App. 1.3

# APPENDIX 2

# SCORE INTERFACE MODULE

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# APPENDIX 2

# SCORE INTERFACE MODULE

## INTRODUCTION

1. The SCORE interface module is an optional internally mounted board which provides for extended or remote control of the receiver using a receiver control unit such as the Racal MA 1075. It also allows two receivers, each fitted with a SCORE interface, to be interconnected for space diversity operation. The SCORE (Serial Control of Racal Equipment) control system is described in the following paragraphs.

## SCORE FORMAT

2. The SCORE format for serial control is designed to cater for numerous applications and contains ample additional capacity for expansion. It is based on a number of 48-bit synchronous frames, each of which contain a 16-bit preamble (synchronisation, word number identification, etc) followed by a 32-bit data word. The total capacity of the system is sixteen 32-bit data words which is equivalent to approximately 400 separate lines. All sixteen words may be revertively checked.

3. Separate lines are used for both data and clock signals travelling in each direction. These comply with RS422/3, and, over short distances, are compatible with RS232/CCITT V28.

4. The SCORE format for the words used by the RA 1792 (word numbers 0, 1, 2 and 5) is given in table 1 (page 4). Although word 0 may be sent as part of a control data sequence, it does not contain any control information and is used only for revertive data.

## ROUTINE AND NEW DATA

5. Under static conditions, i.e. when the control data being transferred from control unit to receiver does not contain change-of-function information, 'routine data' frames are sent in numerical sequence, and at a rate determined by the clock frequency. When a change of function is made however, instead of allowing the transfer of the full sequence of frames to occur before the change of function is executed at the receiver, the next frame to be sent will contain the data word carrying the change of function informaton. Thus the frames are sent out of sequence and priority is given to those frames containing new data. This is achieved under software control where a flag is set each time a control setting is changed to indicate that the appropriate word requires transmission. The flag is reset when the data word is transmitted.

## FRAME COMPARISON

6. Error detection is accomplished by use of the frame comparison technique, which means that two identical frames must be received at the receiver before a change of function can occur. An exception to this is made for the frequency frame (containing word 1), which may be sent singly (new data frames only) by inclusion of external links.

PREAMBLE

7. A 16-bit preamble is added to each 32-bit data word to form one complete 48-bit frame. The preamble contains a 6-bit sync. code, a 2-bit transmit-receive (PTT) code, a control inhibit bit, a return monitor bit, a 2-bit address word security code and a 4-bit data word ident; these are described in the following paragraphs.

Sync. Code

8. The sync. code (bits 0 to 5) consists of a '0' followed by five consecutive '1's. The maximum number of consecutive '1's to occur in serial BCD data is four, e.g. BCD seven followed by BCD eight. This then makes five '1's a unique code. For added security, the next two bits of the preamble (used for PTT) may not consist of two consecutive '1's. This is done to 'terminate' the sync. code and to prevent the generation of a false sync. code following a line break etc.

Transmit/Receive

9. Bits 6 and 7 of the preamble are used for transmit/receive switching (PTT) where the transmit state mutes the receiver and may also set an associated transmitter to the transmit condition. As mentioned in para. 8, these two bits must not consist of consecutive '1's. For the transmit state, bit 6 is set to a '1' and bit 7 is set to '0', whilst for the receive state, bit 6 is set to '0' and bit 7 is set to '1'.

Control Inhibit Bit

10. This bit of the preamble (bit 8) is normally used, as the name implies, to inhibit control of the receiver via the serial control data. When it is set to a '1', the control settings of the receiver remain unchanged and further control instructions conveyed by the 32-bit data words are ignored. The revertive data however, is returned in the normal way, i.e. the receiver settings are returned.

Return Monitor Bit

11. The return monitor bit is normally set to '0' and is only set to '1' to give continuous revertive monitor when single frequency frames are being sent from the control unit (para. 6).

Address Security Code

12. Bits 10 and 11 of the preamble are used in words 8 and 9 of the SCORE control system (equipment and operator addressing words respectively) to provide added security against incorrect addressing. These two bits are set to '0' in all words used by the RA 1792 (and the MA 1075).

Data Word Ident

13. The last four bits of the preamble (bits 12 to 15) are used for the data word identification code, in binary format, i.e. 0 to 15 (decimal) or 0 to F (hexadecimal).

## Table 1: SCORE Data Format

| | BIT NO. | BIT FUNCTION OR FORCED STATE | MONITOR (0) | FREQUENCY (1) | ANALOGUE (2) | HF MODE (5) |
|---|---|---|---|---|---|---|
| PREAMBLE | 0 | 0 | | | | |
| | 1 | 1 | | | | |
| | 2 | 1 SYNC | | | | |
| | 3 | 1 CODE | | | | |
| | 4 | 1 | | | | |
| | 5 | 1 | | | | |
| | 6 | TRANSMIT | | | | |
| | 7 | RECEIVE | | | | |
| | 8 | CONTROL INHIBIT | | | | |
| | 9 | RETURN MONITOR | | | | |
| | 10 | ADDRESS | 0 | 0 | 0 | 0 |
| | 11 | EQUIPMENT | 0 | 0 | 0 | 0 |
| | 12 | 1 DATA | 0 | 1 | 0 | 1 |
| | 13 | 2 WORD | 0 | 0 | 1 | 0 |
| | 14 | 4 IDENT | 0 | 0 | 0 | 1 |
| | 15 | 8 | 0 | 0 | 0 | 0 |
| ...rA WORD | | | MONITOR | FREQUENCY | ANALOGUE | HF MODE |
| | 16 | | A | 1 | 1 | 0 |
| | 17 | | B USER | 2 1 Hz | 2 BFO | 0 NOT |
| | 18 | | C FUNCTION | 4 | 4 x 10 Hz | 0 USED |
| | 19 | | D | 8 | 8 | 0 |
| | 20 | | 0 | 1 | 1 | 0 |
| | 21 | | 0 | 2 10 Hz | 2 BFO | 0 |
| | 22 | | 0 | 4 | 4 x 100 Hz | 0 |
| | 23 | | 0 | 8 | 8 | 0 |
| | 24 | | 0 NOT | 1 | 1 BFO | 0 |
| | 25 | | 0 USED | 2 100 Hz | 2 x kHz | 0 |
| | 26 | | 0 | 4 | 4 | 0 |
| | 27 | | 0 | 8 | BFO SIGN | 0 |
| | 28 | | 0 | 1 | 0 | 1 MODE |
| | 29 | | 0 | 2 kHz | 0 | 2 |
| | 30 | | 0 | 4 | 0 | 4 |
| | 31 | | 0 | 8 | 0 | 0 |
| | 32 | | MUTE | 1 | 0 NOT | SYMMETRICAL |
| | 33 | | FAULT | 2 10 Hz | 0 USED | 0 |
| | 34 | | FC ERROR | 4 | 0 | 0 |
| | 35 | | 0 | 8 | 0 | 0 |
| | 36 | | RF METER | 1 | 0 | AGC DUMP |
| | 37 | | 0 | 2 100 kHz | 0 | 1 |
| | 38 | | 0 NOT | 4 | 0 | 2 AGC |
| | 39 | | 0 USED | 8 | 1 | 4 |
| | 40 | | 1 | 1 | 2 | 1 |
| | 41 | | 2 | 2 MHz | 4 IF | 2 BANDWIDTH |
| | 42 | | 4 | 4 | 8 GAIN | 4 |
| | 43 | | 0 METER READING | 8 | 0 | 0 |
| | 44 | | 8 | 1 10 MHz | 16 | W |
| | 45 | | 16 | 2 | 32 | X USER |
| | 46 | | 32 | 1 SINGLE FRAME | 64 | Y FUNCTION |
| | 47 | | 64 | 2 CHECK BITS | 128 | Z |

DATA WORDS

14. As stated in para. 4, words 0, 1, 2 and 5 are used by the RA 1792. These are described in the following paragraphs which should be read in conjunction with table 1. Certain words contain a number of 'forced zeros' to prevent the possible occurrence of five consecutive '1's which would otherwise be mistaken for a sync. code.

WORD 0 - MONITOR

15. This word is used for revertive signalling only; although it may be transmitted as part of a forward control data sequence, it does not contain any control data.

User Functions

16. The first four bits of data word 0 provide for the revertive user functions where up to four earth (0 V) signals applied to the receiver are reproduced at rear panel connections of the control unit. The four bits are labelled A, B, C and D, and correspond with the A, B, C and D connections at both the receiver and control unit.

Revertive Indications

17. The next operative bits of word 0 are bits 32, 33 and 34. Bit 32 is set to a '1' when a mute signal is applied to the receiver, and this is conveyed to the control unit via the revertive data to illuminate the MUTE indicator on the control unit front panel. Data bit 33 (the fault bit) is set to a '1' following a fault condition in the synthesizer section of the RA 1792 receiver, and this condition is conveyed to the control unit via the revertive data to illuminate the FAULT indicator on the control unit front panel. Data bit 34 is the frame comparison error bit and is normally at '0'; it goes to a '1' when three consecutive frame comparison errors are detected at the receiver, and this also results in the illumination of the FAULT indicator.

RF Metering

18. Data bit 36 is set to a '1' to select RF metering, and the RF meter reading data is conveyed, in 7-bit digital format, via data bits 40 to 42 and 44 to 47 (bit 43 is a forced zero).

WORD 1 - FREQUENCY

19. The first 30 bits of this word (16 to 45 inclusive) contain the frequency setting information in BCD format. The remaining two bits (46 and 47) determine whether frame comparison is required (for error detection), in which case each frame is sent twice, or whether single frequency frames are to be sent.

WORD 2 - ANALOGUE

20. Word 2 contains the analogue functions, BFO and IF gain. For a receiver set for local control, the range of the BFO is between plus 8 kHz and minus 8 kHz (centred on 455 kHz). For remote control however, the maximum offset is restricted to the range plus and minus 7.79 kHz i.e. three data bits (24, 25 and 26) are used for the kHz digit (giving a maximum figure of 7), and to prevent the generation of a spurious sync. code, data bit 23 must not be set to a '1' (thus giving a maximum figure of 7 for the 100 Hz digit). Data bit 27 is the BFO sign bit and is set to a '1' for negative BFO offset frequencies, to a '0' for positive BFO offset frequencies.

21. The receiver manual IF gain control data is conveyed between control unit and receiver via data bits 39 to 42 and 44 to 47 (bit 43 in a forced zero). This gain control data is not however, transferred from master receiver to slave receiver when two receivers are interconnected for space diversity operation. In this case the receiver diversity AGC outputs are interconnected.

WORD 5 - HF MODE

22. This word is used for mode, AGC and bandwidth selection, and for the forward user functions.

Mode

23. Bits 28 to 32 inclusive are concerned with mode selection. The state of bit 32 determines whether a symmetrical mode or a sideband mode is selected, as shown in the following table.

| BCD coding of Bits 28 to 31 | Bit 32 State | Mode Selected | |
|---|---|---|---|
| 1 | 1 | AM | } Symmetrical |
| 2 | 1 | CW | |
| 5 | 1 | FM | |
| 0 | 0 | USB | } Sideband |
| 1 | 0 | LSB | |
| 2 | 0 | ISB-U | |
| 3 | 0 | ISB-L | |

AGC

24. Bit 36 is used for AGC dump; when set to a '1' it causes a rapid decay of the AGC voltage level so that the level may be re-established for the signal being received. The coding of bits 37, 38 and 39 in given below.

| BCD Code | Function |
|---|---|
| 0 | Manual and short |
| 1 | Manual and medium |
| 2 | Manual and long |
| 3 | Manual only |
| 4 | Short |
| 5 | Medium |
| 6 | Long |
| 7 | Not allowed |

Bandwidth

25. The coding of bits 40 to 42 is given below. The actual filters fitted are dependent upon the particular receiver options. The filter numbers given correspond with those on the receiver main IF/AF board.

| BCD Code | Filter No. |
|---|---|
| 0 | Not Used |
| 1 | Not Used |
| 2 | 3 (Narrowest Bandwidth) |
| 3 | 4 |
| 4 | 5* |
| 5 | 6 |
| 6 | 7 |
| 7 & 8 | Not Used |

* May select filter 2 if offset sideband filter.

User Functions

26. The last four bits of word 5 provide for the forward user functions where up to four earth (0 V) signals applied to the receiver control unit are reproduced at rear panel connections on the RA 1792 receiver. The four bits are labelled W, X, Y and Z and correspond with the similarly marked input and output connections of the control unit and receiver respectively.

REVERTIVE DATA

27. The format of the revertive data is the same as for the control data. Frame comparison however, does not take place, and the revertive data is generally sent in single frames.

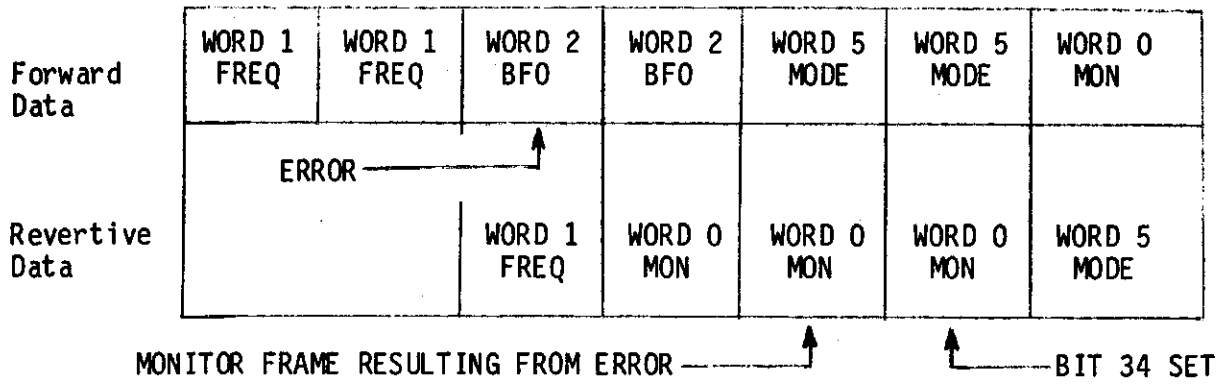
28. Provided that the control inhibit and return monitor bits of the forward data preamble are not set to a '1', that single frequency frames are not being sent, and that no errors occur in the control data, then the form of the revertive data is given by the following example.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Forward Data | WORD 0 MON | WORD 0 MON | WORD 1 FREQ | WORD 1 FREQ | WORD 2 BFO | WORD 2 BFO | WORD 5 MODE |
| Resulting Revertive Data | | WORD 0 MON | WORD 0 MON | WORD 0 MON | WORD 1 FREQ | WORD 0 MON | WORD 2 BFO |

29. In this example, the forward data consists of two word 0 frames, two word 1 frames, two word 2 frames and the first of two word 5 frames. Since two frames have to be sent and compared before any action can take place, the revertive data resulting from the forward data given in this example is shown lagging the forward data by two 48-bit frames (ignore for the moment the first revertive data word 0). The two forward data word 0 frames are compared; since no bit errors are present, the two frames are identical and a word 0 frame is returned. The next frame comparison however, is between a word 0 and a word 1. The comparison is therefore unsuccessful, and, although an error does not exist, it is arranged to send back a word 0 monitor frame. Two word 1 frames are now compared, and result in a revertive word 1 frame. The next comparison is between a word 1 frame and a word 2 frame, which results in a revertive word 0 frame, two word 2 frames result in a revertive word 2 frame, and so on. The control of the first (blank) revertive data frame is dependent on the previously sent data, whilst the next frame (the first word 0 frame in this example) must be a word 0 frame due to a comparison between two disimilar frames. Note that when two RA 1792 receivers are interconnected for master/slave operation, word 0 control data frames are not sent by the master receiver.

Frame Comparison Error

30. A frame comparison error signal is generated only on the failure of three consecutive frame comparisons, as shown in the following example:




31. In this example the forward data consists of two word 1 frames, two word 2 frames, two word 5 frames and the first of a pair of word 0 frames. The two frequency word frames result in a revertive frequency word frame and the next two frames (frequency and BFO) result in a monitor word 0 frame. The two BFO word frames are compared, and this time, due to an error, the frame comparison is unsuccessful, resulting in a further revertive monitor frame. The next two frames (BFO and mode) being disimilar also result in a revertive monitor frame. Thus three consecutive revertive monitor frames result following the FAILURE of three consecutive frame comparisons; a frame comparison error signal is generated and this is conveyed by bit 34 of the revertive word 0 frame.

Control Inhibit

32. If the control inhibit bit (bit 8 of the preamble) in a forward control data frame is set to a '1', and provided that the return monitor bit (bit 9 of the preamble) is not set to a '1', then the revertive data frames are sent in pairs and in numerical sequence and convey the actual receiver setting data.

Return Monitor

33. If the return monitor bit (bit 9 of the preamble) in a series of forward control data frames is set to a '1', then the revertive data consists of a series of continuous monitor frames.

CLOCK CIRCUITS

34. These provide the timing signals required by the various parts of the system. The basic data rate clock signal may be generated either by an external unit, such as a modem, or may be provided by an internal clock generator (approximately 6 kHz).

SIGNAL-TO-LINE REQUIREMENTS

35. The RA 1792 receiver signal-to-line requirements for the serial data and clock signals comply with EIA standards RS-422 and RS-423. The SCORE clock and data output drivers are configured for RS-422, a differential balanced voltage interface which is fully compatible with CCITT recommendations V11 and X27. The maximum permissible line length is dependent on factors such as data signalling (clock) rate, tolerable signal distortion and noise interference. In general, the maximum line length at a data signalling rate of 100 k bauds is 1200 metres (4000 ft), reducing to approximately 15 metres (50 ft) at the maximum data signalling rate of 10 M bauds. Note however, that the maximum data signalling rate for the RA 1792/MA 1075 is 9.6 k bauds. If no connection is made to the RS-422 positive output, a single ended interface suitable to drive an RS-232 receiver is produced, provided the line length does not exceed 15 metres (50 ft).

36. The line receivers used for the SCORE clock and data input signals comply with EIA standards RS-422 (balanced voltage interface) and RS-423 (unbalanced voltage interface). When connected for an unbalanced transmission line (positive input terminal grounded), the circuit may be driven from a single-ended RS-232 driver circuit provided the line voltages do not exceed plus and minus 12 V. A comparison of the specifications for EIA standards RS-232, RS-422 and RS-423 (as far as the RA 1792 is concerned) is given in table 2, and the noise immunity figures for mixed single-ended interfaces are given in table 3.

Table 2: Comparison of Specifications

| CHARACTERISTICS | RS-232C (CCITT V28) | RS-423 | RS-422 |
|---|---|---|---|
| Mode | Single Ended | Single Ended | Differential |
| Logic '1' (OFF State) | Negative Voltage | Negative Voltage | Negative Voltage |
| Logic '1' (ON State) | Positive Voltage | Positive Voltage | Positive Voltage |
| Maximum Line Length | 15 m (50 ft) at 20 k Bauds | 1200 m (4000 ft) at 3 k Bauds | 1200 m (4000 ft) at 100 k Bauds |
| Maximum Data Rate | 20 k Bauds | 300 k Bauds | 1 M Bauds |
| Open Circuit Driver Voltage (maximum) | ± 25 V | ± 6 V | ±6 V differential |
| Loaded Driver Voltage (minimum) | ±5 V to ±15 V | ±3.6 V | 2 V differential |
| Driver Output Load - Power Off | 300 ohms | 100 µA (-6 V to +6 V) | 100 µA 6 V to 0.25 V |
| Driver Short - Circuit Current | ±500 mA | ±150 mA | ±150 mA |
| Driver Slew Rate | 30 V/µ second | Capacitor controlled | Not restricted |
| Receiver Input Resistance | 3 k ohms to | Equal to or greater than 4k ohms | Equal to or greater than 4k ohms |
| Receiver Threshold | -3 V to +3 V | -0.2 V to +0.2 V | -0.2 V to +0.2 V |
| Maximum Receiver Input Voltage | ±25 V | ±12 V | ±12 V |

Table 3: Noise Immunity

| DRIVER | RECEIVER | NOISE IMMUNITY (MINIMUM) |
|---|---|---|
| RS-232C | RS-232C | 2 V |
| RS-423 | RS-423 | 3.4 V |
| RS-232C | RS-423 | 4.8 V |
| RS-423 | RS-232C | 0.6 V |

37. The remaining external input and output connections to and from the SCORE interface conform to a common convention. Logic input signals are defined as follows:

Logic '1' - ON state: Steady state short-circuit current to 0 V, less than 40 mA.
Logic '0' - OFF state: Internally pulled up to a positive voltage, usually +12 V (for C-MOS).

38. Logic output signals are defined as follows:

Logic '1' - ON state: representd by a short circuit to 0 V via a current-saturated open-collector transistor.
Logic '0' - OFF state: represented by the open-circuit output from a transistor in the cut-off condition i.e. the externally applied open-collector pull-up voltage (up to +20 V).

INSTALLATION

39. Detailed installation information is beyond the scope of this appendix and reference should be made to the appropriate system manual. Typical interconnection diagrams are however given for a space diversity installation using a pair of RA 1792 receivers (Fig. App. 2.1) and for a remote control installation using the MA 1075 receiver control unit (Fig. App. 2.2).

SCORE INTERFACE BOARD
FUNCTIONAL DESCRIPTION

40. The following functional description should be read in conjunction with the block diagram of the SCORE interface board given in fig. App. 2.3. When the unit is switched on, the initialisation routine resets the receive interrupt latch ( /10 READ, 10C3 and 10C7 applied to the address decoder), resets the transmit interrupt latch (I/O port 1 bit 1) and enables the receive and transmit interrupt circuitry (via PIO port 84, bits 6 and 7).

SCORE Receiver

41. Inverted SCORE control data (from another RA 1792 receiver or a receiver control unit) is clocked into a sync. code detector and, via an inverter,

to an 8-bit serial in/parallel and serial out shift register. When a correct inverted sync. code is detected, a strobe pulse is generated which is applied to:

(1) the reset input of an 8-bit counter.

(2) the strobe input of the shift register; the data in each shift register stage is transferred to a storage register and will appear at the parallel outputs when a '1' is applied to the enable input.

(3) the set input of the receiver interrupt latch; the output changes to a '1' and this causes the peripheral input/output (PIO) device to generate an interrupt signal which is routed to the microcomputer (via the control bus).

42. The microcomputer examines the receive and transmit interrupt pending lines, decides that a receive interrupt has occurred, and then applies address 88 (IOC3 and IOC7), together with the /IO READ Signal to the address decoder. The resulting '1' output resets the receive interrupt latch and enables the 8-bit shift register to route the first 8 bits of the received frame (bits 0 to 7 of the preamble) to the microcomputer via the processor data bus.

43. Successive bytes of received SCORE control data are transferred in a similar manner except that the strobe pulses are produced by the 8-bit counter instead of the sync. code detector i.e. the Q4 output from the 8-bit counter is applied to the set input of the strobe pulse generator, and reset is applied after the CR time constant.

44. The serial control data output from the shift register (delayed by eight clock periods) is routed via an inverter to a rear panel socket (Data out external) for connection to an external unit using the SCORE extra word facility (see Fig. App. 2.1(a)).

SCORE Transmitter

45. The SCORE transmit shift register receives parallel SCORE data frames (words 0, 1, 2 and 5) from the microcomputer (I/O port 0) or serial data frames (external revertive data from an external unit using the extra word facility) and transmits this SCORE data in serial form. For a remote control installation, revertive data resulting from received control data is transmitted back to the receiver control unit, whilst for the master/slave situation using a pair of RA 1792 receivers, the forward control data is transmitted from the control receiver to the slave receiver, or revertive data from the slave receiver is transmitted back to the master receiver.

46. At the end of the last but one byte of a SCORE data frame handled by the SCORE receiver, the microcomputer applies a start-in-sync. set pulse to the timing and control circuitry of the SCORE transmitter. This causes the generation of a load pulse which is used to produce the following:

(1) A clock signal for the transmit interrupt latch; the '0' at the D input results in a '1' at the $\overline{Q}$ output which is routed to the interrupt control circuit and via an inverter to the microcomputer (I/O power 1).

(2) The parallel/serial control signal for the output shift register; if the next SCORE frame to be transmitted contains word 0, 1, 2 or 5, then the microcomputer sets line 6 of PIO port 85 to a '1' and the output shift register is set to receive parallel data from the microcomputer. If however, the next frame to be transmitted does not contain a word used by the receiver, then the output shift register is set to receive external serial revertive data (from an external unit using the extra word facility).

(3) A reset signal for an 8-bit counter. This reset signal is maintained until the end of the next load pulse (which is produced by the Q4 output signal from the SCORE receiver 8-bit counter). The two 8-bit counters are then synchronised and successive load pulses are then produced by the SCORE transmitter 8-bit counter. Counter synchronisation becomes relevant should gaps occur during successive received data frames (para. 62).

47. The Q4 output from the 8-bit counter is also applied to the clock input of the external probe pulse generator. The D input of this stage is controlled by the microcomputer and is only set to a '1' following successful frame comparison of the received SCORE data. The external strobe pulse is then produced and is applied to the external extra word unit to enable the revertive data output.

SCORE Data Input and Output Timing

48. Fig. App. 2(a) shows a typical situation where an RA 1792 receiver is controlled by an MA 1075 control unit, and an extra-word control unit (using SCORE word 7) connected to the MA 1075 controls an external unit connected to the RA 1792. Pairs of SCORE control data frames containing words 0, 1, 2 and 5 are produced by the MA 1075, and pairs of word frames are inserted into the control data stream from the MA 1075 on request by the extra word control unit. The revertive data from the SCORE word 7 controlled unit consists of 40-bit words from bit 8 to bit 47 i.e. the sync code (bits 0 to 7) is not included.

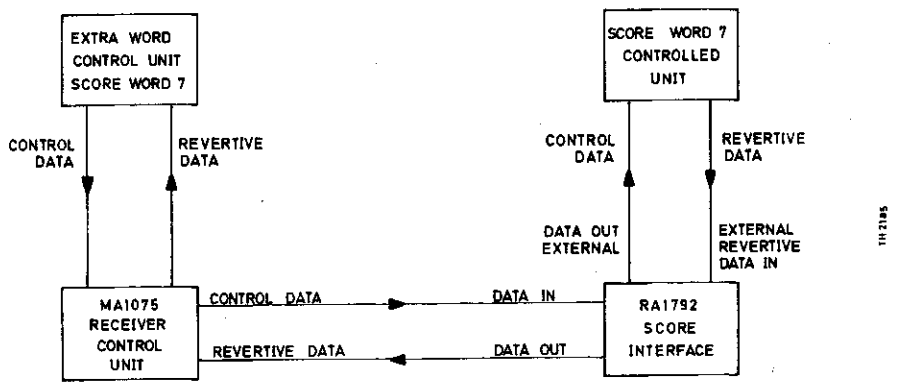



Fig. App. 2 (a) SCORE Data Routing

49. The timing diagram given in fig. App. 2(b) relates to fig. App. 2(a) and shows the SCORE data input and output timings as far as the RA 1792 SCORE interface is concerned. The DATA IN comprises a pair of word 7 frames (originating from the extra word control unit), two word 1 and two word 2 frames (from the MA 1075), two further word 7 frames, and the first of a pair of word 5 frames (from the MA 1075). This data is clocked into an 8-bit shift register and is then applied to the microcomputer in parallel bytes. It is also clocked out of the register in serial form for application to the SCORE word 7 controlled unit (DATA OUT EXTERNAL), delayed by eight clock periods due to the action of the shift register.

50. The microcomputer frame-compares the first word 7 frame with the last frame received, and since the two frames do not compare, a SCORE word 0 revertive data frame is produced (DATA OUT). the data content of the first DATA OUT frame shown in Fig. App. 2(b), marked X, is the result of the previous frame comparison. The next frame comparison undertaken by the microcomputer is between two word 7 frames, and in this example, successful frame comparison is assumed (if the comparison had failed, a further revertive word 0 frame (DATA OUT) would have been produced).

51. The microcomputer also examines the word identification bits of each DATA IN frame. Following the successful frame comparison between a pair of frames not used by the RA 1792 i.e. the word 7 frames in this example, a sync. code is loaded into the SCORE transmit output shift register, and the register is then set to allow a serial input. The external strobe pulse is then produced and applied to the SCORE word 7 controlled unit. This responds by applying the revertive 40-bit word 7 data to the SCORE interface where it is clocked into and straight out of the SCORE transmit output shift register, preceded by the sync. code inserted by the microcomputer. This revertive word 7 frame is then routed via the MA 1075 to the extra word control unit.

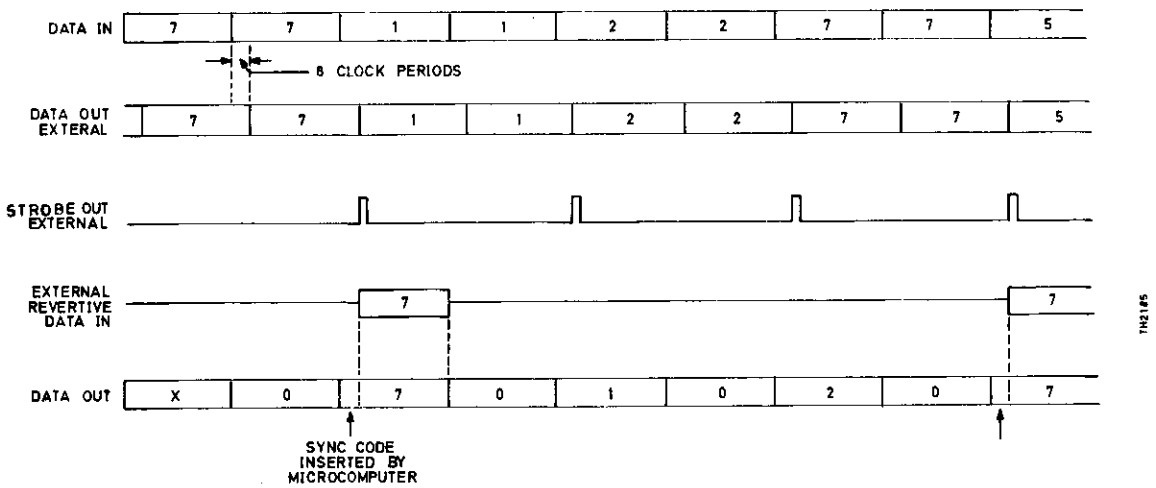



Fig. App. 2(b) Timing Diagram : SCORE Data

52. The next frame comparison takes place between a word 7 frame and a word 1 frame, and this results in a revertive (DATA OUT) word 0 frame. Two word 1 frames are then successfully compared, a word 1 frame is returned, and an external strobe pulse is generated. This pulse is applied to the SCORE word 7 controlled unit but because a further pair of word 7 frames have not been received, no revertive data is available and the strobe pulse has no effect.

User Functions

53. The input and output user functions are handled by a peripheral input/output (PIO) device which interfaces to the microcomputer via two high-speed I/O ports, designated 84 and 85, and a control bus. The frame comparison inhibit input is also routed to the microcomputer via I/O port 85 (bit 7).

CIRCUIT DESCRIPTION (Fig. App. 2.4)

SCORE RECEIVER
Sync. Code Detector

54. The inverted SCORE input data (RS-423 or RS-232) is applied via a line receiver, U3A, to the D input of a 4-bit shift register U13B, and via inverter U14D to the D input of an 8-bit shift register U23 (para. 57). The Q3 output of U13B is applied to the reset input of a further 4-bit shift register U13A, where the D input is connected to +5 V (logic '1'). Data is shifted into these registers on the positive-going transition of the SCORE clock signal from line receiver U3B.

55. When an inverted sync. code is received i.e. 1-0-0-0-0-0-X-X, it takes three clock pulses for the first '1' to reach the Q3 output of U13B; this holds U13A in the reset state for the duration of the next clock pulse, and a further four clock pulses are required before the Q4 output of U13A changes to a '1' (table 4). Thus the Q4 output of U13A can only change to a '1' following the occurrence of five consecutive zeros at the D input of U13B. This circuit does not detect the state of the last two bits of the received sync-code but this is subsequently checked by the system software. The '1' at the Q4 output of U13A is applied to the clock input of the strobe pulse generator U10A via glitch suppression components R2, C8.

Table 4: Sync. Code Detector

| SHIFT REGISTER STATES | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| U13B | Q1 | 1 | 0 | 0 | 0 | 0 | 0 | X | X |
| | Q2 | X | 1 | 0 | 0 | 0 | 0 | 0 | X |
| | Q3 | X | X | 1 | 0 | 0 | 0 | 0 | 0 |
| | Q4 | X | X | 0 | 1 | 0 | 0 | 0 | 0 |
| U13A | Q1 | X | X | 0 | 0 | 1 | 1 | 1 | 1 |
| | Q2 | X | X | 0 | 0 | 0 | 1 | 1 | 1 |
| | Q3 | 0 | X | 0 | 0 | 0 | 0 | 1 | 1 |
| | Q4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

X = 0 or 1

Strobe Pulse Generator

56. The strobe pulse generator comprises D-type flip-flop U10A. When clocked by the output from the sync. code detector, the '1' at the D input is transferred to the Q output, and reset is applied after the time constant presented by R1 and C7. The nominal 5 microsecond positive-going output pulse is applied to:

(1) The set input of the receiver interrupt latch U10B; the resulting '1' at the Q output is applied to NAND gate U15A of the interrupt control circuit (para. 64), and via inverting buffer U14A to the microcomputer as the receive interrupt pending signal.

(2) The strobe input of the 8-bit shift register U23 to load the internal storage latches with the first eight bits (the sync. code) of the received frame (para. 57).

(3) The reset input of an 8-bit counter U11A; this counter produces a positive-going pulse at the Q4 output for every eight SCORE clock cycles following reset, and these pulses are applied to the set input of U10A to produce the strobe pulses for the remaining five bytes of the received data frame. The Q4 output of ML11a is also routed to NAND gate U16A which forms part of the output counter synchronisation circuit (para. 59).

Input Shift Register

57. U23 is an 8-stage serial shift register having a storage latch associated with each stage. The data in each shift stage is transferred to the storage register when a '1' is applied to the strobe input, and the stored data appears at the O1 to O8 parallel output when a '1' is present at the enable input. When a '0' is present at the enable input, the O1 and O8 outputs are in the high-impedance 3-state condition. The serial output is taken from the Q's pin (where it appears eight clock periods after application to the D input) and is routed to J1 pin 2 via open-collector inverter Q5.

Address Decoder

58. The address decoder makes use of three transmission gates (analogue switches) U21b, U21c, and U21d. For a SCORE read operation, the microcomputer sets the IOC3 and IOC7 control bus lines to a '1' and the I/O read line to a '0'. U21A is thus held off, U21B and U21C are turned on, and a '1' from R16 is applied to the enable input of the 8-bit shift register U23, and the parallel data at the Q1 to Q8 output pins is applied to the micrcomputer via the processor data bus. The '1' from U21C is also applied to the reset input of the receive interrupt latch U10B, the Q output is reset to '0', and the receive interrupt is cancelled.

SCORE TRANSMITTER
Start-in-Sync. Latch

59. The start-in-sync. latch U22A is reset by the micrcomputer during the initialisation routine (I/O port 1 bit 0) and is set by the micrcomputer shortly after the start of the last byte of a SCORE data frame handled by the SCORE receiver (I/O port 1 bit 3). The $\overline{Q}$ output of U22A is thus set

to a '0', this is routed to NAND gate U16B and the '1' output resets the 8-bit counter U11B. At the same time the Q output of U22A is set to a '1'; the combination of this and the next positive-going pulse from the SCORE receive 8-bit counter U11A (at the end of the last byte of a received data frame - see timing diagram fig. App. 2(c)), results in a '0' at the output of NAND gate U16A. This is inverted by NAND gate U16D and a '1' is applied to the set input of the load pulse generator U17B.

Load Pulse Generator

60. The load pulse generator U17B is set either by the action of the start-in-sync. latch (as described in para. 59) or subsequently by the Q4 output of the 8-bit counter (via U14E and U16D). In either case, U17B is effectively reset by the next negative-going transition of the SCORE clock, which is applied via inverter U14B (D input at 0 V), and thus the positive and negative-going pulses at the Q and $\overline{Q}$ outputs extend for one half of a SCORE clock period.

61. With reference to the timing diagram given in Fig. App. 2(c), the first and last load pulses shown (U17B outputs) result following the Q4 output of the 8-bit counter U11B. The positive-going pulse at the Q output of U17B is applied to the clock input of the internal/external latch U17A (para. 66) and also to the clock input of the start-in-sync. latch U22A; this however, has no effect as the Q output of U22A is already at logic '0'. The negative-going pulse at the $\overline{Q}$ output of U17B is inverted by U16B to reset the 8-bit counter U11B. It is also applied to NAND gate U16C, which forms part of the parallel/serial selection circuit for the output shift register (para. 66), and to the clock input of the transmit interrupt latch U22B. Thus at the positive going transition of the negative-going pulse, the '0' at the D input of U22B results in a '1' at $\overline{Q}$ output; this is routed to the microcomputer via inverter U14F as a transmit interrupt pending signal, and is also applied to NAND gate U15D which forms part of the interrupt control circuitry (para. 64). The positive-going transition of the negative-going pulse from the $\overline{Q}$ output of U17B is also used to clock the output enable latch U12B (para. 68).

62. The second load pulse shown in Fig. App. 2(c) results from the combination of a '1' at the Q output of the start-in-sync latch U22A and the positive-going output pulse from the 8-bit counter U11A. This time, the positive-going pulse at the Q output of U17B clocks the internal/external latch U17A as before, but also clocks the start-in-sync. latch U22A. The '0' at the D input is transferred to the Q output, is inverted by U16A, and a '1' is thus applied to U16D to allow load pulse generation by the Q4 output signals from the 8-bit counter U11B (applied to the set input of U17B via U14E and U16D). The negative-going pulse at the $\overline{Q}$ output of U17B extends the reset period of U11B for the duration of the pulse and then allows counting to commence so that the first Q4 output pulse from U11B occurs exactly eight SCORE clock periods after the previous Q4 output pulse from 8-bit counter U11A, i.e. synchronism between the two 8-bit counters is established.

63. Synchronisation between the two 8-bit counters is necessary due to the asynchronous nature of the received SCORE data, as illustrated in Fig. App. 2(d). This shows an example three-clock-period delay between the last byte of one frame and the first byte of the next frame. In this case, the first byte of data transferred to the microcomputer does not constitute a correct sync code, and the data is rejected. Three clock periods later however, the sync. code detector detects the presence of a

correct sync. code, a strobe pulse is produced, and the 8-bit counter U11A (which has reached a count of 3) is reset to zero and starts again. The example 3-bit delay is then automatically transferred to the output 8-bit counter U11B by the action of the synchronisation circuit.

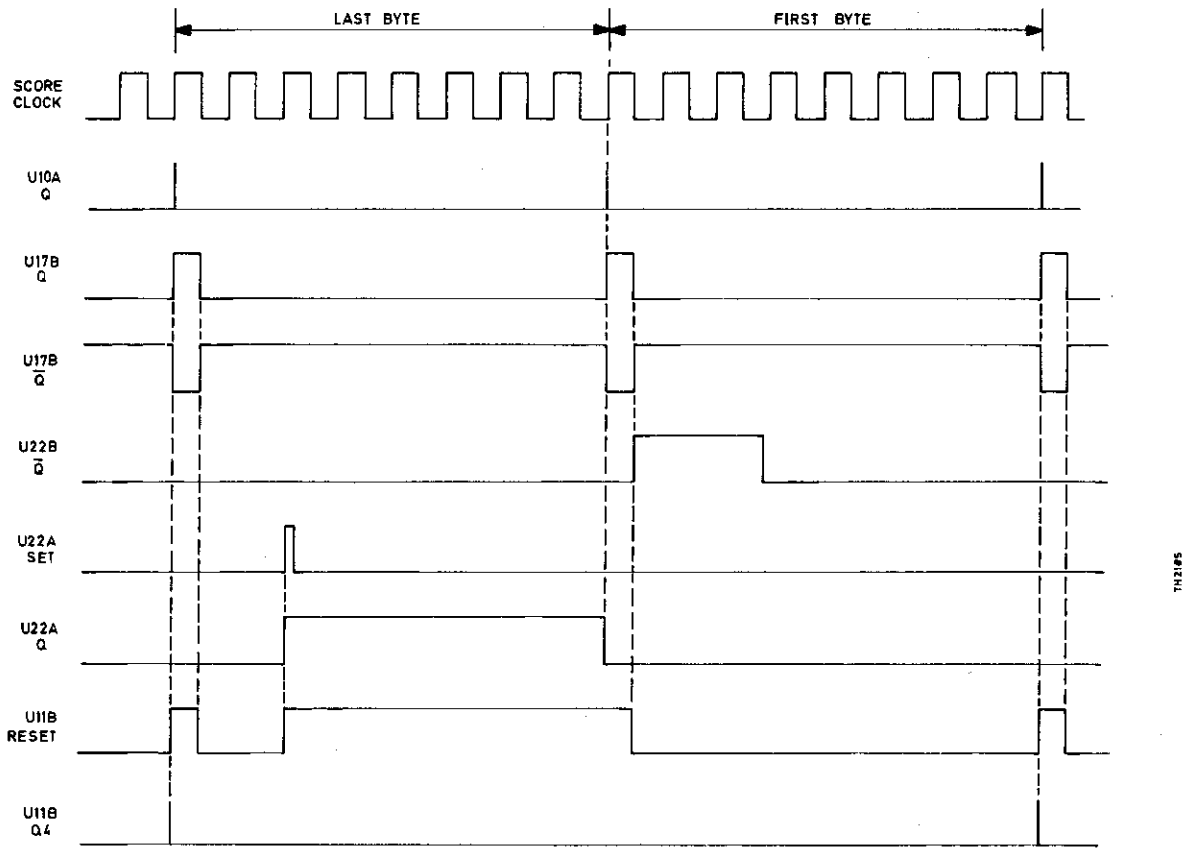



Fig. App. 2(c) Timing Diagram : Counter Synchronisation

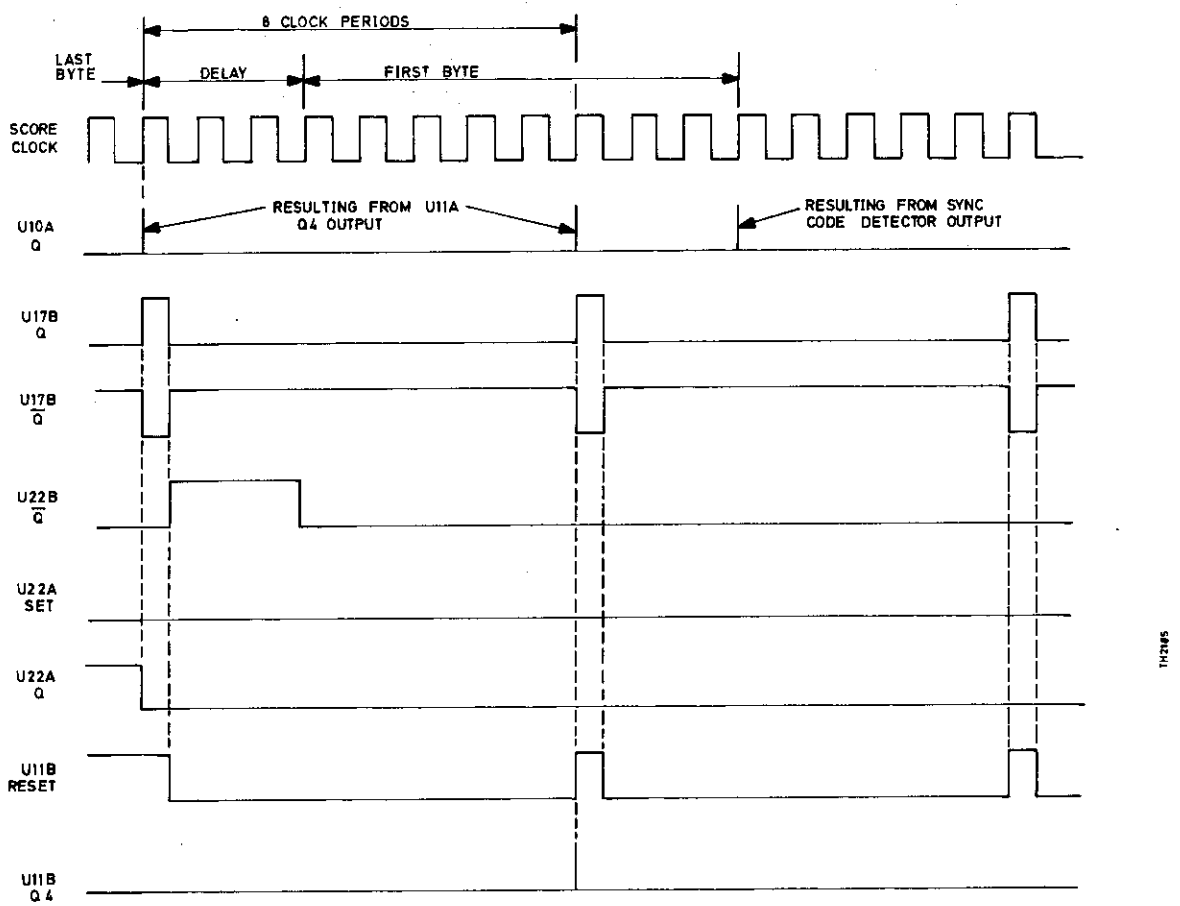



Fig. App. 2(d) Timing Diagram : Delayed SCORE Data

## Interrupt Control

64. The Logic '1' output signals from the receive and transmit interrupt latches, U10B and U22B respectively, are gated (U15A, U15D) with the respective software - controlled interrupt enable signal from U19 (I/O port 84, bits 6 and 7). The resulting '0' output from either U15A or U15D is inverted by U15C and applied to one input of U15B. Provided an interrupt request from elsewhere within the receiver is not being serviced, then a '0' is present at P1 pin 28 ($\overline{ICB}$ input); this is applied to the priority in input of U19 to enable the interrupt circuitry, and is inverted by U14B to allow the output from U15C to produce a logic '0' external interrupt request signal, which is applied to the microcomputer, and also applies a mask-programmed interrupt vector address (hex 0680) to the microcomputer via the processor data bus. The microcomputer is then forced to execute the interrupt routine pointed to by the vector address 0680. Whilst the interrupt routine is in progress, the priority out output from U19 is set to logic '1'; this is applied to the priority in input of the static memory interface (SMI) device in the microcomputer to prevent that device from initiating an interrupt.

External Strobe

65. The external strobe pulse generator U12A is clocked by the Q4 output from the 8-bit counter U11B. When an external strobe pulse is required, the microcomputer routes a '1' to the D input of U12A (strobe enable), this is transferred to the Q output on the positive-going transition of the Q4 output pulse from U11B, and U12A is reset after the time constant presented by R3, C12. The resulting positive-going pulse is inverted by open-collector transistor Q7 and is taken to J1 pin 21 for connection to equipment using the extra word facility.

Internal/External Data Control

66. The output shift register U24 is configured under software control to accept either parallel data from the microcomputer (via I/O port 0) or serial external revertive data at J1 pin 14 (applied to U24 via CR6 and inverting NAND buffer/driver U7B). For internal (parallel) input data operation, the microcomputer routes a '1' to the D input of the internal/external latch U17A; this is transferred to the Q output on the positive-going transition of the positive-going load pulse from U17B, transmission gate U21A is enabled, and the path between I/O port 0 bit 0 and the P8 input of U24 is completed. At the same time the negative going load pulse from U17B is inverted by U16C to momentarily enable the parallel inputs of U24, the parallel data is loaded in, and is then serially clocked out.

67. For external (serial) input data operation, the microcomputer routes a '0' to the D input of U17A; this time U21A is not enabled, the path between I/O port 0 bit 0 and the P8 input of U24 is broken, and U16C applies to '1' to U24 to enable the parallel inputs. The external revertive data is applied to the P8 input of U24 and is then serially clocked out.

68. The SCORE data and clock output driver U9 is enabled by the application of a '0' at pin 3. When the RA 1792 receiver is switched on, the initialisation routine latches a '1' at U19 I/O port 84 bit 5. This is routed to the D input of the output enable latch U12B, and after the first load pulse from U17B, a permanent '0' is established at the $\overline{Q}$ output. The '1' at the Q output is applied to open collector transistor Q9, but in the RA 1792 no connection is made to J1 pin 1.

PERIPHERAL INPUT/OUTPUT (PIO) DEVICE

69. The PIO device U19 is mainly used for interrupt control purposes but is also used for the input output user function information. The device has two input/output ports, logic to handle an external interrupt (para. 64) and a programmable interval timer (which is not used in this application).

An 8-bit bi-directional data bus is used for the transfer of data between the PIO and the microcomputer, and a 5-bi bus (ROMC0 to ROMC4) is used for control purposes. A block diagram of the device is given in Fig. App. 2(e).

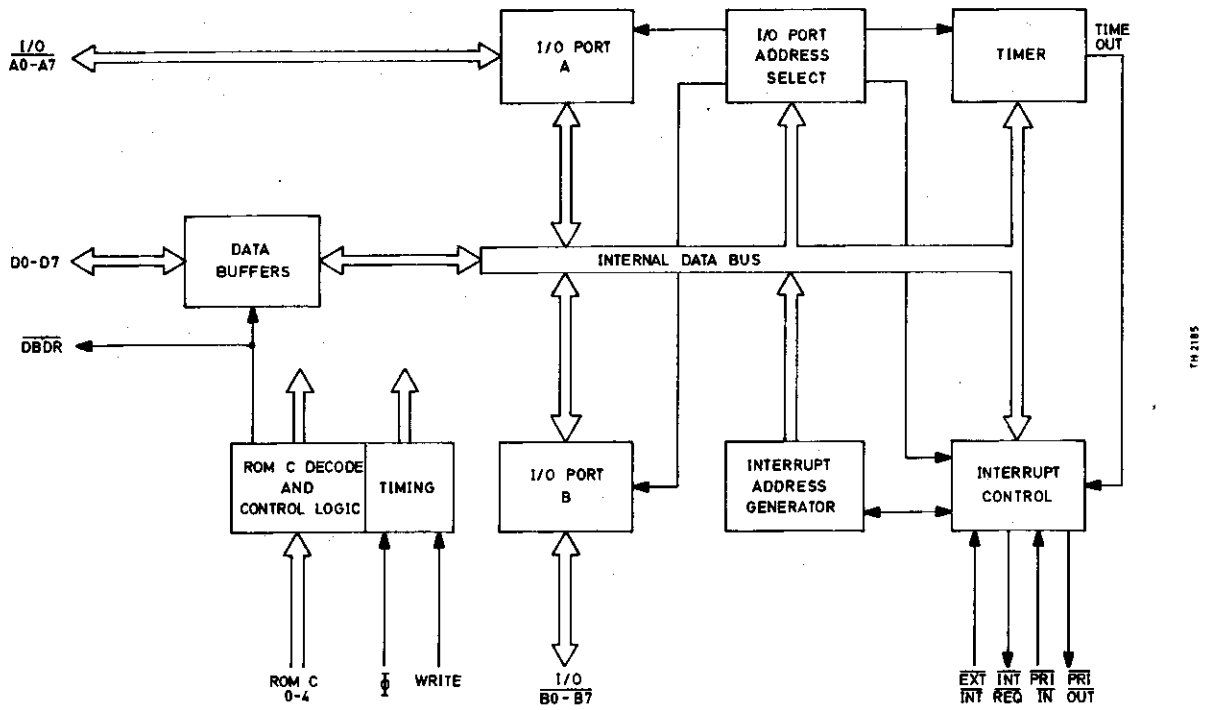



Fig. App. 2(e) Block Diagram : 3861 PIO

70. The PIO device has four addressable ports, each with an assigned address. Two ports are used as 8-bit input/output ports (designated A and B in fig. App. 2(e)), whilst the remaining two ports are for the programmable timer and interrupt control purposes. The designated port addresses for the version of the 3861 PIO used in this application are in the range 04 to 07, as listed in Table 5. These addresses are however, modified by the action of the control bus (ROMC) decoder (para. 75) so that the PIO responds to addresses in the range 84 to 87. Note that the timer and interrupt control ports are write only ports i.e. the contents of the associated port registers cannot be read by the microcomputer.

Table 5: PIO PORT ADDRESES

| Address | | | | Assigned To |
|---|---|---|---|---|
| Physical | | Virtual | | |
| Hex | Binary | Hex | Binary | |
| 04 | 00000100 | 84 | 10000100 | I/O Port A |
| 05 | 00000101 | 85 | 10000101 | I/O Port B |
| 06 | 00000110 | 86 | 10000110 | Interrupt Control Register |
| 07 | 00000111 | 87 | 10000111 | Programmable Timer |

Device Connections

71. (1) Ø and WRITE: These are clock input signals derived by the microcomputer.

(2) ROMC0 to ROMC4: These are the control input signals from the microcomputer.

(3) DB0 to DB7: The bi-directional data bus lines which link the PIO to the microcomputer.

(4) $\overline{\text{EXT INT}}$: External interrupt input. When an external circuit applies a '0' to this input, an external interrupt request is latched into the PIO provided the interrupt control register has been set to allow external interrupts. The PIO subsequently communicates this interrupt request to the microcomputer via the $\overline{\text{INT REQ}}$ line.

(5) $\overline{\text{PRI IN}}$: Priority in .A'1' at this input denotes that a higher priority peripheral has a pending interrupt request. If the PIO receives an interrupt request, it is latched into the PIO but will not be serviced until a '0' is present at the $\overline{\text{PRI IN}}$ input.

(6) $\overline{\text{PRI OUT}}$: Priority out. This output signal is routed to the $\overline{\text{PRI IN}}$ input of the static memory interface unit in the microcomputer module. A '1' on this line denotes that the PIO has a pending interrupt request.

(7) $\overline{\text{INT REQ}}$: Interrupt request. A logic '0' on this output lines is output to the microcomputer to initiate the interrupt routine.

(8) $\overline{\text{DBDR}}$: Data bus drive. This output goes to a '0' whenever the PIO is driving the data bus as an output. This output is not used in this application.

(9) $\overline{\text{I/O A0-A7}}$ & $\overline{\text{I/O B0-B7}}$: Two bi-directional 8-bit input/output ports, A and B. In this application these ports respond to addresses 84 and 85 respectively.

Control Bus

72. The control bus, comprising the five lines labelled ROMC0 to ROMC4, conveys control signals to the PIO and also to the static memory interface (on the microcomputer board). The ROMC states decoded by the PIO are given in Table 5. Note that all ROMC states not listed in table 6 are decoded as 'no-operation'.

Instruction Execution

73. The microcomputer input/output instructions place the required I/O port address on the processor data bus during one instruction cycle, and then use the processor data bus in the following instruction cycle to carry out the actual I/O data transfer. The ROMC lines from the microcomputer (hex. states 1A and 1B) signal the PIO that an I/O data movement is occurring during the current instruction cycle. Thus for ROMC I/O transfer states 1A and 1B (table 5) the PIO requires to know whether the contents of the data bus during the previous instruction cycle matched any of the four assigned I/O addresses. This is accomplished by the I/O port address selection logic which constantly monitors the data bus. When an address match is detected, the information is held through the following instruction cycle.

74. Read instructions that select a port (addresses 84 and 85) cause the contents of the selected port to be placed on the processor data bus during the read instruction cycle. For write instructions, the PIO accepts a byte from the processor bus and loads it into one of the I/O ports or the interrupt control register (the programmable timer is not used in this application). Each I/O port output line is latched and thus holds the data transferred during the last I/O write instruction.

Table 6: DECODED ROMC STATES

| ROMC STATE | | PIO |
|---|---|---|
| HEX | BINARY | FUNCTION |
| 0F | 01111 | If an interrupt request is pending and $\overline{\text{PRI IN}}$ is at '0', the lower half of the interrupt vector address (80) is placed on the data bus. |
| 10 | 10000 | Place interrupt circuitry in an inhibit state that prevents altering the interrupt chain. |

| ROMC STATE | | PIO |
|---|---|---|
| HEX | BINARY | FUNCTION |
| 13 | 10011 | If an interrupt request is pending and $\overline{\text{PRI IN}}$ is at '0', the upper half of the interrupt vector address (06) is placed on the data bus and the interrupt circuit is reset. |
| 1A | 11010 | If an I/O port address was present on the data bus during the previous instruction cycle, move current contents of data bus into the appropriate port (I/O A, I/O B, timer or interrupt control). |
| 1B | 11011 | If I/O port address 84 or 85 was present on the data bus during the previous instruction cycle, move contents of appropriate I/O port (I/O A or I/O B) onto the data bus. |

Control Bus Decoder

75. The control bus decoder consists of a magnitude comparator U20 and a quad transmission gate U25. It monitors the ROMC control bus lines and when the 03 state is present, it inverts the level present on the PB7 processor data bus line which is applied to the PIO (U19 pin 7). Thus when an address in the range 84 to 87 is present on the processor data bus, it appears at the PIO data bus as an address in the range 04 to 07, i.e. the physical address range of the four PIO ports. The action of the circuit is as follows.

76. The magnitude comparator U20 produces a '1' at the A=B output when the logic levels at the A inputs are equal to these at the B inputs, and a '1' is also present at the A=B input. Thus when ROMC lines 0 and 1 are both at '1' and lines 2 to 4 are at '0' (03 code), a '1' is produced at the A=B output. This enables U25A and U25C, the '0' from U25A disables U25B, and the level present at the PB7 data bus line is inverted by U25D before application to pin 7 of U19 via U25C. For any other ROMC code, the A=B output of U20 is at '0', U25A and U25C are disabled, and U25B is enabled to connect the PB7 data bus line directly to pin 7 of U19.

77. The microcomputer applies 03 to the ROMC lines each time a PIO port address is applied to the data bus. As far as the PIO device is concerned, ROMC state 03 is a 'no-operation' (para. 72).

USER FUNCTIONS

78. The input user functions are applied to the PIO (I/O port 85) via inverting buffer/drivers U5A, U5B, U6A and U6B. The output user functions from the PIO (I/O port 84) are routed to rear panel connector J1 via open-collector inverters Q1 to Q4. The new data output request signal from Q8 is not used in this application.

INTERNAL CLOCK GENERATOR

79. This uses the otherwise spare section of the quad line receiver U3C. R15 is selected on test to produce a squarewave output at approximately 6 kHz.

-5 V SUPPLY

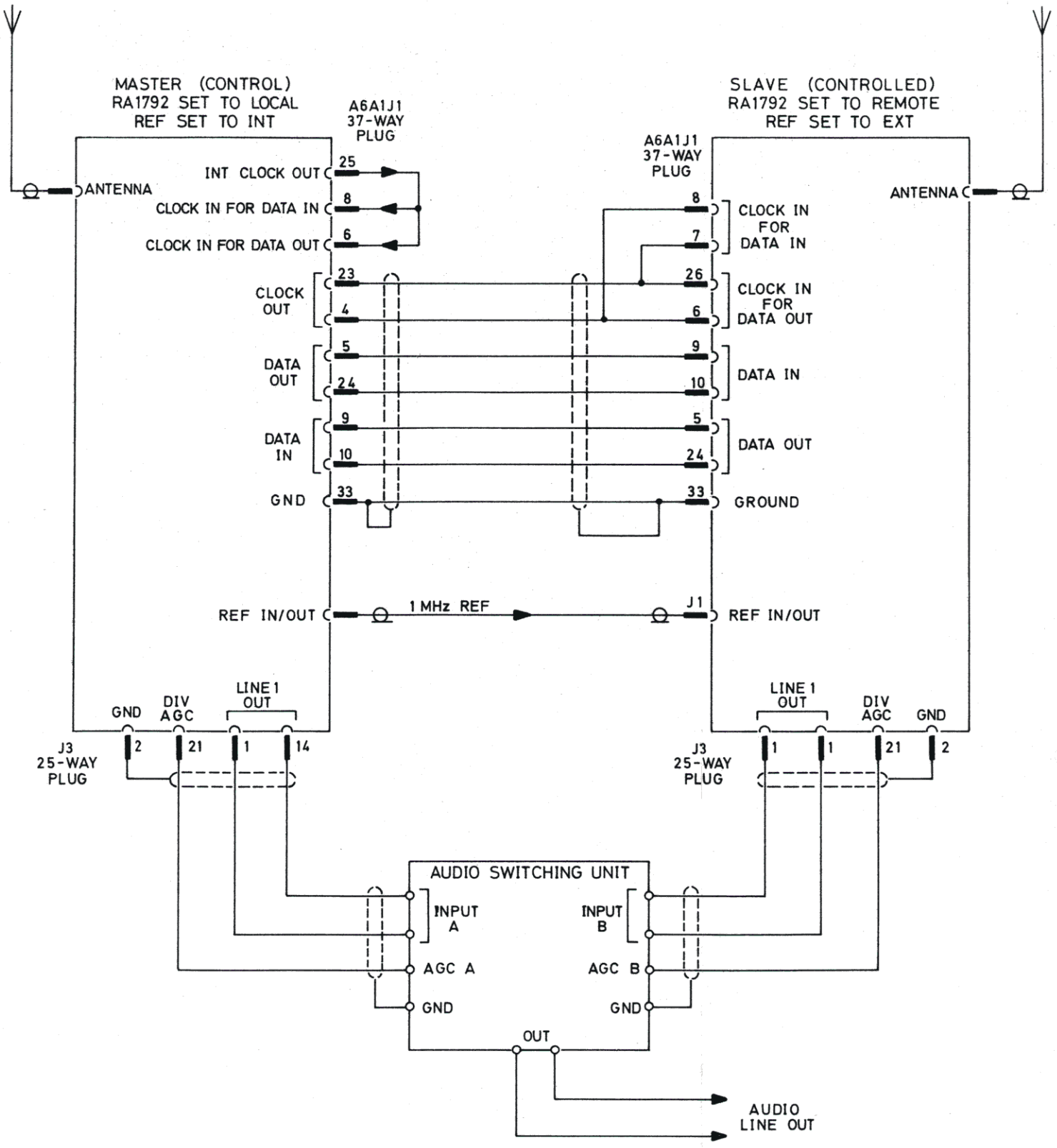
80. The -5 V supply required by the line driver device U9 is provided by three-terminal regulator U18 which is powered from the -15 V supply at P1 pin 23.

## SCORE INTERFACE BOARD (ST 08459)

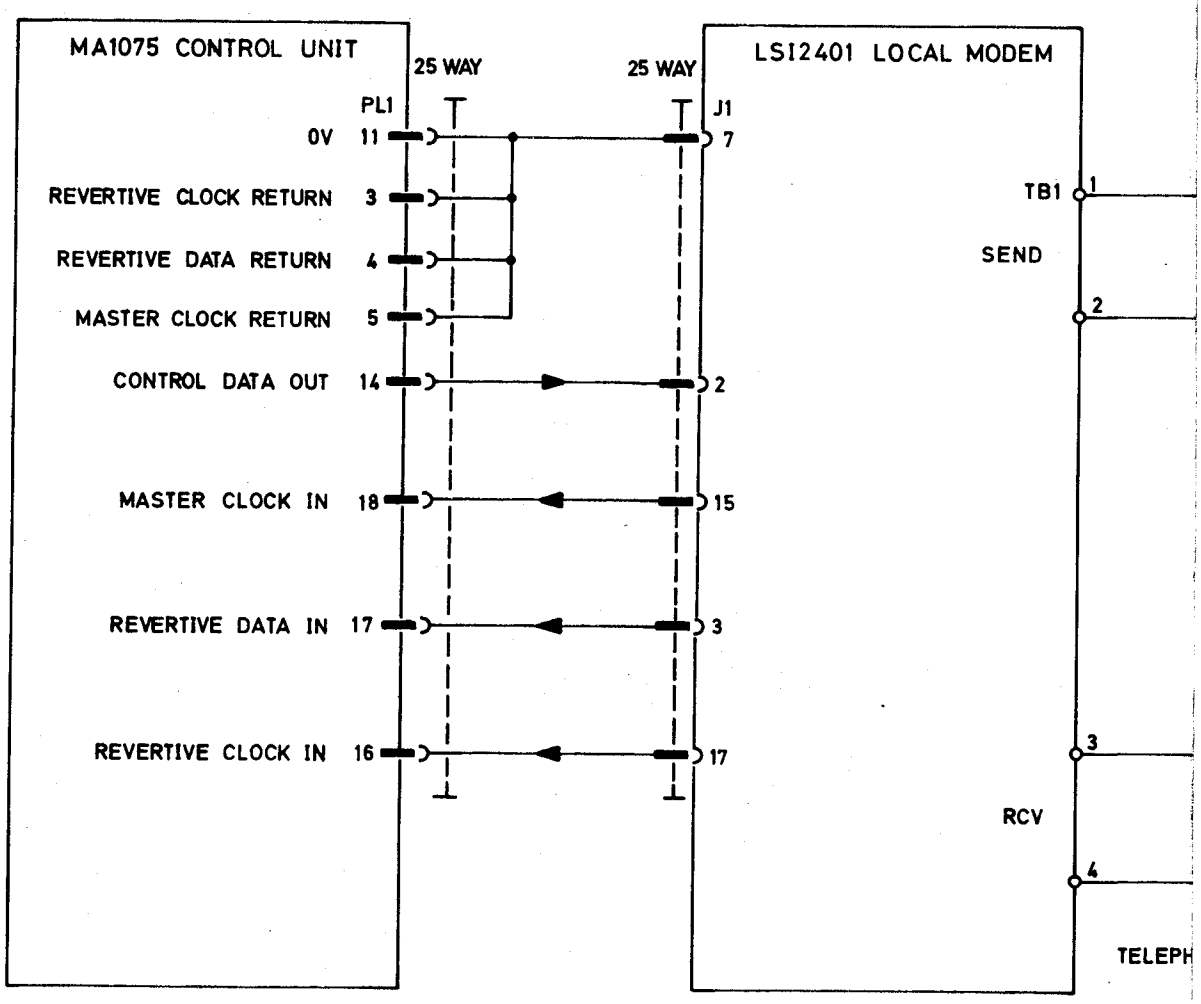
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | W | | |
| R1 | 68 k | Metal Oxide | ¼ | 2 | 916478 |
| R2 | 68 k | Metal Oxide | ¼ | 2 | 916478 |
| R3 | 68 k | Metal Oxide | ¼ | 2 | 916478 |
| R4 | 68 k | Metal Oxide | ¼ | 2 | 916478 |
| R5 | 68 k | Metal Oxide | ¼ | 2 | 916478 |
| R6 | | Not Used | | | |
| R7 | 22 k | Metal Oxide | ¼ | 2 | 913493 |
| R8 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R9 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R10 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R11 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R12 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R13 | 15 k | Metal Oxide | ¼ | 2 | 920645 |
| R14 | 33 k | Metal Oxide | ¼ | 2 | 913495 |
| R15 | 15 k to 56 k | Selected on test | | | |
| R16 | 1 k | Metal Oxide | ¼ | 2 | 913489 |
| R17 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R18 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R19 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| R20 | 10 k | Metal Oxide | ¼ | 2 | 914042 |
| **Capacitors** | | | V | | |
| C1 | 0.1 | Disc Ceramic | 50 | 20 | 938406 |
| C2 | 0.22 | Disc Ceramic | 50 | 20 | 928676 |
| C3 | .01 | Disc Ceramic | 50 | 20 | 938053 |
| C4 | 22 | Tantalum | 10 | 20 | 921090 |
| C5 | 6.8 | Tantalum | 20 | 20 | 938031 |
| C6 | 6.8 | Tantalum | 20 | 20 | 938031 |
| C7 | 100 p | Disc Ceramic | 500 | 10 | 938556 |
| C8 | 47 p | Disc Ceramic | 500 | 10 | 917418 |
| C9 | 47 p | Disc Ceramic | 500 | 10 | 917418 |
| C10 | 47 p | Disc Ceramic | 500 | 10 | 917418 |
| C11 | 47 p | Disc Ceramic | 500 | 10 | 917418 |
| C12 | 100 p | Disc Ceramic | 500 | 10 | 938566 |
| C13 | .01 | Disc Ceramic | 50 | 20 | 938053 |
| C14 | 47 p | Disc Ceramic | 500 | 10 | 917418 |

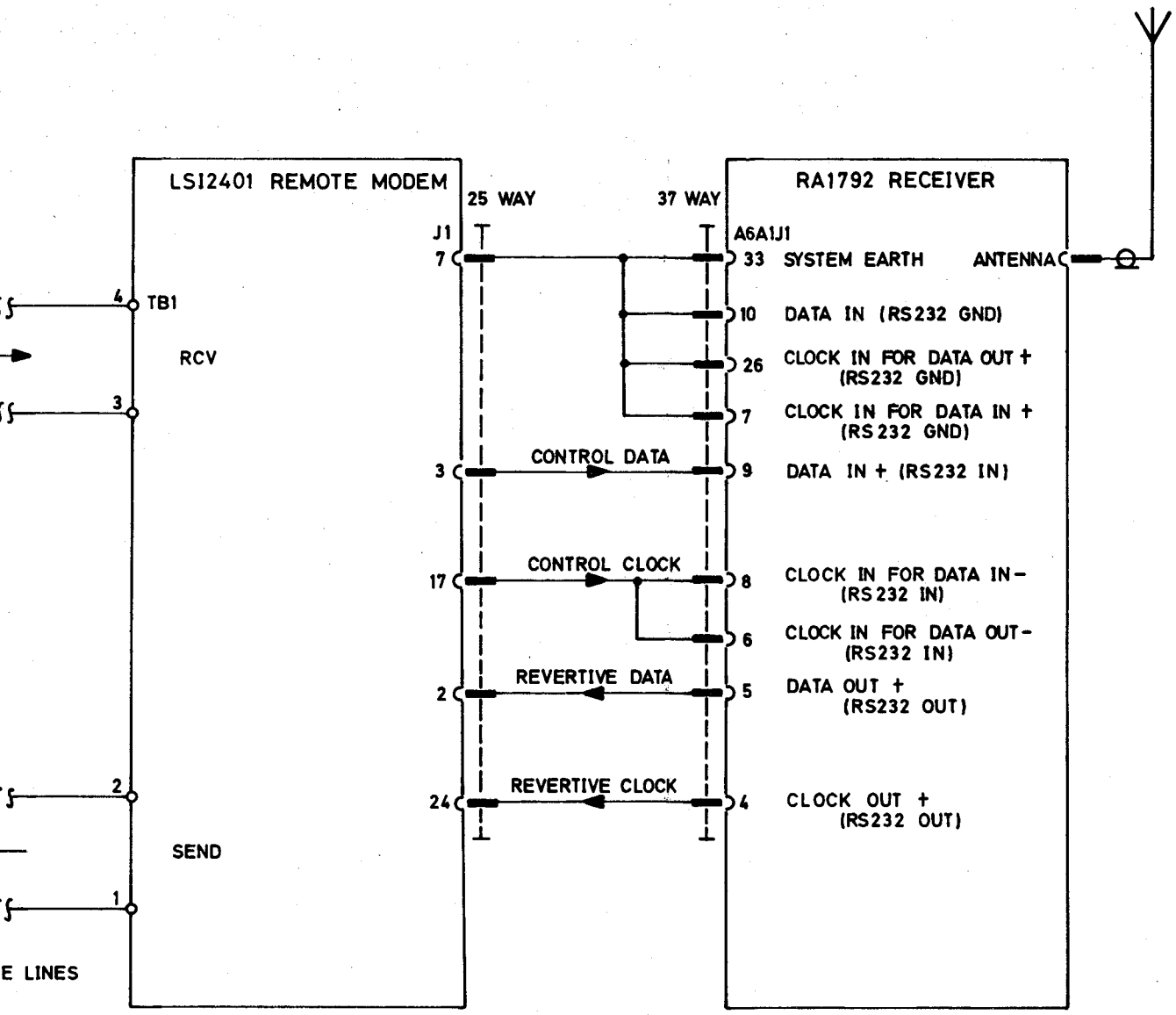
| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Connectors** | | | | | |
| J1 | | Socket 37-way | | | 938678 |
| | | Mating plug, 37-way | | | 916507 |
| | | Shell, junction | | | 918105 |
| | | Retainer | | | 914245 |
| P1 | | Plug, 50-way PCB | | | A07881 |
| | | Comprising: | | | |
| | | Connector, Right Angle, 25-way | | | 938689 |
| | | Connector, Right Angle, 25-way | | | 938690 |
| **Diodes** | | | | | |
| CR1 | | Silicon 1N916 | | | 913480 |
| CR2 | | Silicon 1N916 | | | 913480 |
| CR3 | | Silicon 1N916 | | | 913480 |
| CR4 | | Silicon 1N916 | | | 913480 |
| CR5 | | Silicon 1N916 | | | 913480 |
| CR6 | | Silicon 1N916 | | | 913480 |
| CR7 | | Silicon 1N916 | | | 913480 |
| CR8 | | Silicon 1N916 | | | 913480 |
| **Transistors** | | | | | |
| Q1 | | NPN Silicon 2N3904 | | | 914046 |
| Q2 | | NPN Silicon 2N3904 | | | 914046 |
| Q3 | | NPN Silicon 2N3904 | | | 914046 |
| Q4 | | NPN Silicon 2N3904 | | | 914046 |
| Q5 | | NPN Silicon 2N3904 | | | 914046 |
| Q6 | | NPN Silicon 2N3904 | | | 914046 |
| Q7 | | NPN Silicon 2N3904 | | | 914046 |
| Q8 | | NPN Silicon 2N3904 | | | 914046 |
| Q9 | | NPN Silicon 2N3904 | | | 914046 |
| **Integrated Circuits** | | | | | |
| U1 | 10 k | Resistor Network, SIL | | | 933750 |
| U2 | 68 k | Resistor Network, DIL | | | 938680 |
| U3 | | Quad line receiver 26LS32 | | | 938683 |
| U4 | | Not used | | | |
| U5 | | Dual 2-input NAND buffer 40107 | | | 931052 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| U6 | | Dual 2-input NAND buffer 40107 | | | 931052 |
| U7 | | Dual 2-input NAND buffer 40107 | | | 931052 |
| U8 | | Dual 2-input NAND buffer 40107 | | | 931052 |
| U9 | | Dual RS422 line driver 26LS30 | | | 938684 |
| U10 | | Dual D-type flip-flop 4013 | | | 926860 |
| U11 | | Dual BCD Up-Counter 4518 | | | 928002 |
| U12 | | Dual D-type flip flop 4013 | | | 926860 |
| U13 | | Dual 4-bit shift register 4015 | | | 930973 |
| U14 | | Hex inverting buffer 4049 | | | 930033 |
| U15 | | Quad 2-input NAND gate 4011 | | | 920028 |
| U16 | | Quad 2-input NAND gate 4011 | | | 920028 |
| U17 | | Dual D-type flip flop 4013 | | | 926860 |
| U18 | | -5 V 3-terminal regulator 79M05 | | | 938679 |
| U19 | | PIO 3861A | | | 938687 |
| U20 | | Magnitude Comparator 4585 | | | 938686 |
| U21 | | Quad transmission gate 4066 | | | 930148 |
| U22 | | Dual D-type flip-flop 4013 | | | 926860 |
| U23 | | 8-Stage Shift register 4094 | | | 929324 |
| U24 | | 8-Stage Shift register 4014 | | | 930972 |
| U25 | | Quad transmission gate 4066 | | | 930148 |
| U26 | 22 k | Resistor network SIL | | | 938682 |

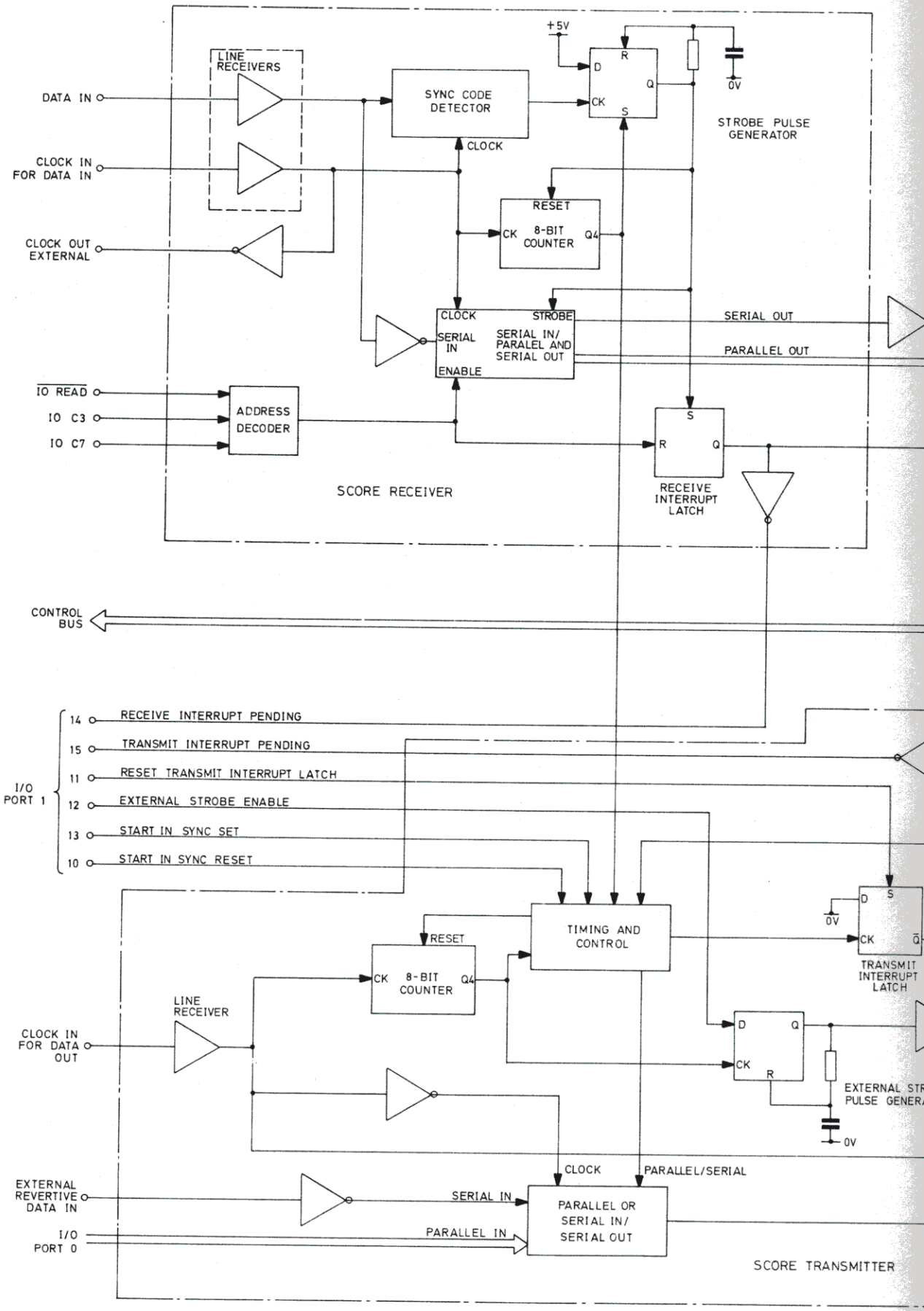


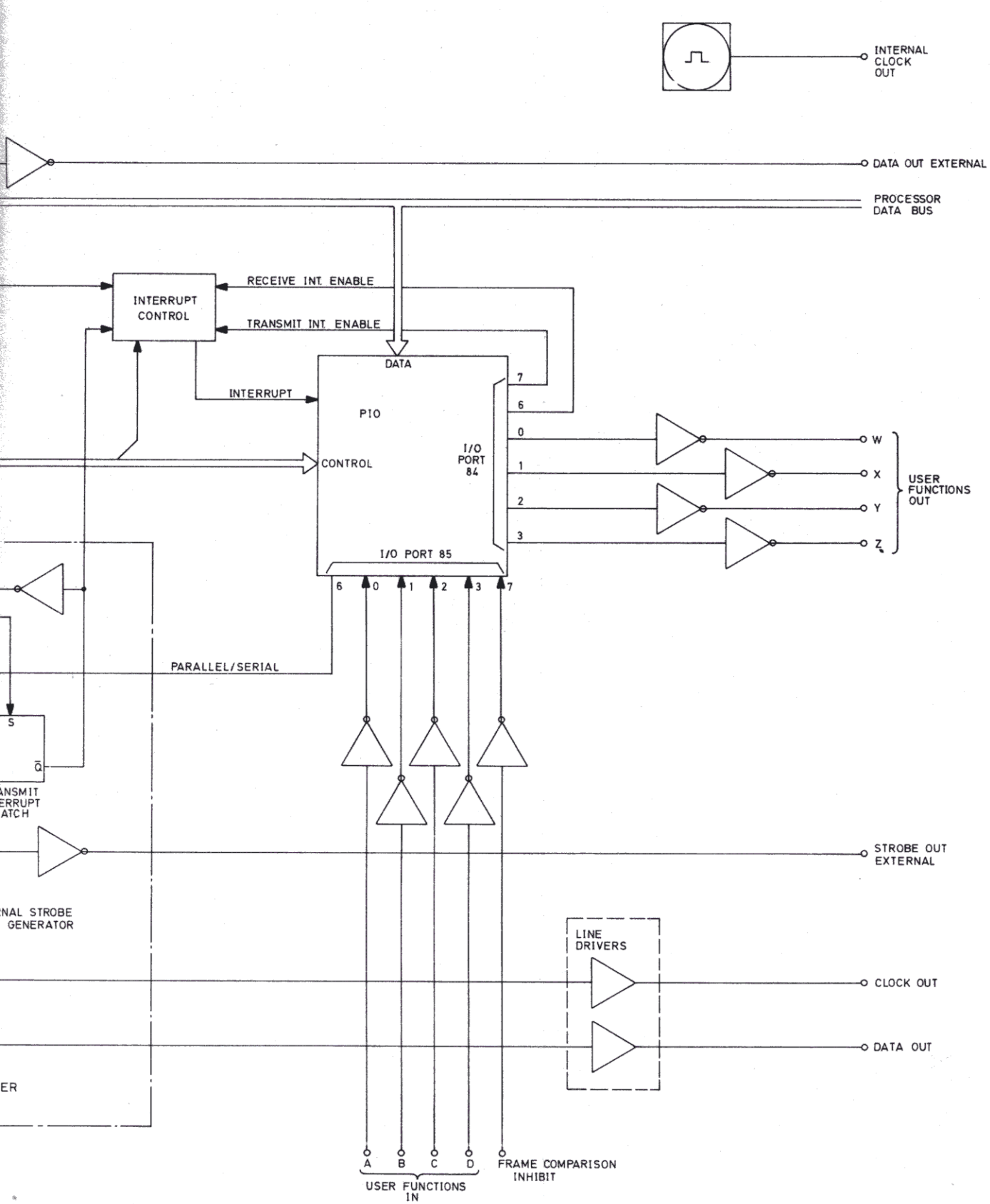

Interconnection Diagram : Typi
Space Diversity Installation Fig


MA1075 CONTROL UNIT
25 WAY
PL1
0V 11
REVERTIVE CLOCK RETURN 3
REVERTIVE DATA RETURN 4
MASTER CLOCK RETURN 5
CONTROL DATA OUT 14
MASTER CLOCK IN 18
REVERTIVE DATA IN 17
REVERTIVE CLOCK IN 16
25 WAY
J1
7
2
15
3
17
LSI2401 LOCAL MODEM
TB1
1
SEND
2
3
RCV
4
TELEPH

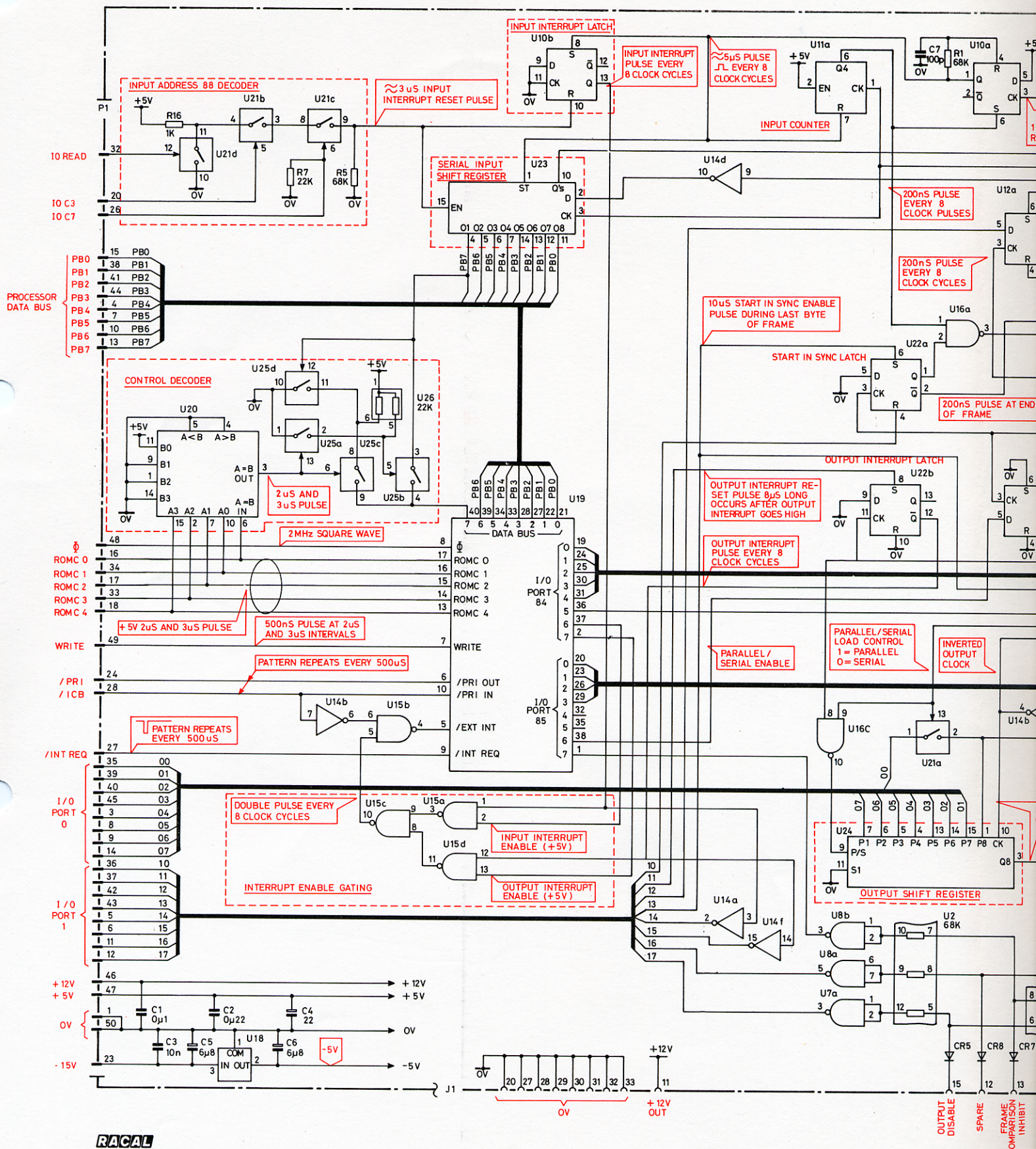



Interconnection Diagram : Typical
Remote Control Installation Fig. App.2.2


+5V
LINE RECEIVERS
DATA IN
CLOCK IN FOR DATA IN
CLOCK OUT EXTERNAL
SYNC CODE DETECTOR
CLOCK
D
R
Q
CK
S
0V
STROBE PULSE GENERATOR
RESET
CK 8-BIT COUNTER Q4
CLOCK
STROBE
SERIAL IN
SERIAL IN/ PARALEL AND SERIAL OUT
ENABLE
SERIAL OUT
PARALLEL OUT
IO READ
IO C3
IO C7
ADDRESS DECODER
S
R
Q
RECEIVE INTERRUPT LATCH
SCORE RECEIVER
CONTROL BUS
I/O PORT 1
14 RECEIVE INTERRUPT PENDING
15 TRANSMIT INTERRUPT PENDING
11 RESET TRANSMIT INTERRUPT LATCH
12 EXTERNAL STROBE ENABLE
13 START IN SYNC SET
10 START IN SYNC RESET
TIMING AND CONTROL
TRANSMIT INTERRUPT LATCH
LINE RECEIVER
CLOCK IN FOR DATA OUT
EXTERNAL STR PULSE GENER
EXTERNAL REVERTIVE DATA IN
I/O PORT 0
CLOCK
PARALLEL/SERIAL
SERIAL IN
PARALLEL IN
PARALLEL OR SERIAL IN/ SERIAL OUT
SCORE TRANSMITTER

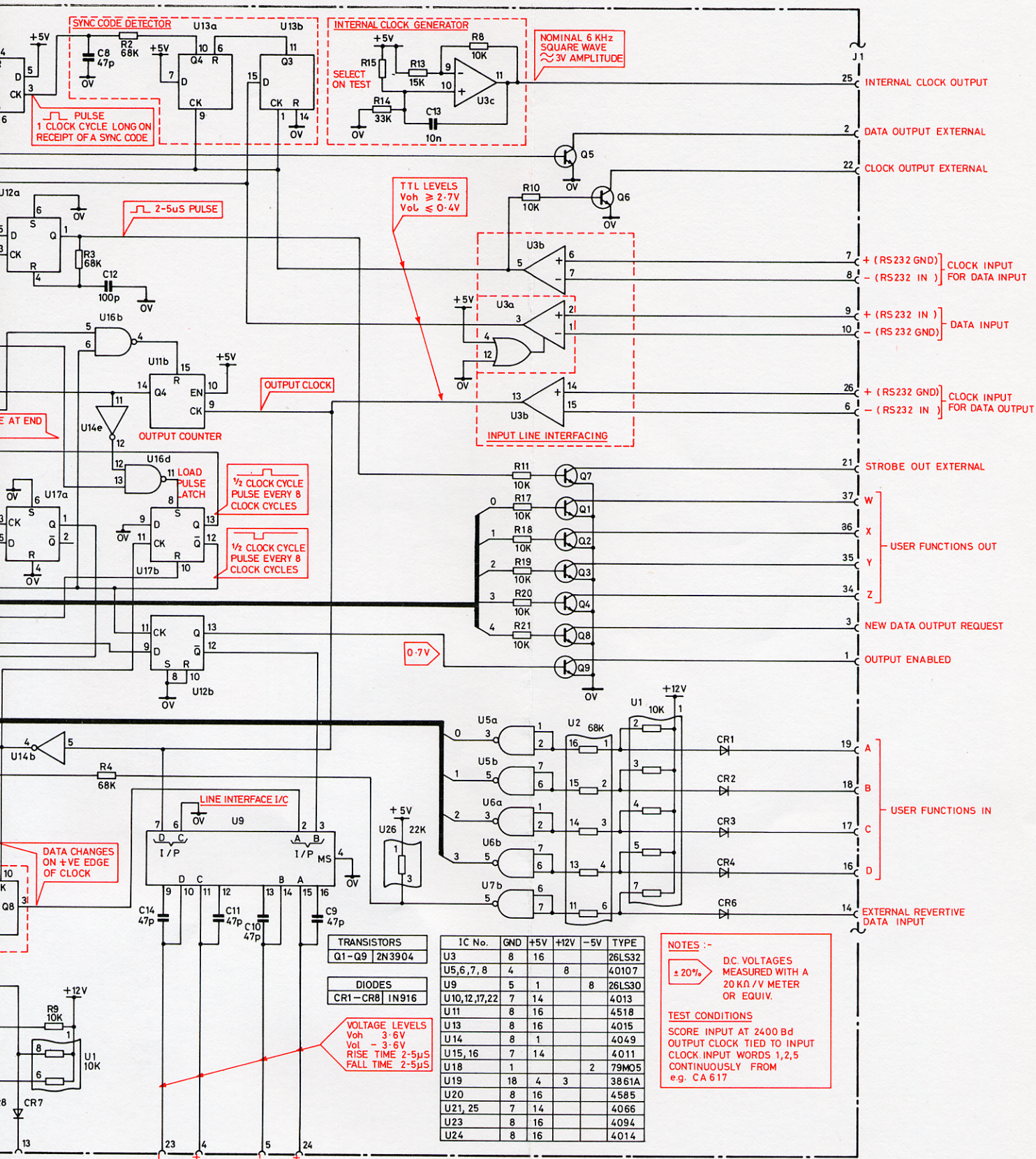



**Block Diagram :**
**SCORE Interface Board** **Fig. App 2.3**




RACAL

| TH3416 | DC08458/1 | TH3416 | DC08458/2 |
|---|---|---|---|
| 5 | 7 | 5 | 7 |




| IC No. | GND | +5V | +12V | -5V | TYPE |
|---|---|---|---|---|---|
| U3 | 8 | 16 | | | 26LS32 |
| U5,6,7,8 | 4 | | 8 | | 40107 |
| U9 | 5 | 1 | | 8 | 26LS30 |
| U10,12,17,22 | 7 | 14 | | | 4013 |
| U11 | 8 | 16 | | | 4518 |
| U13 | 8 | 16 | | | 4015 |
| U14 | 8 | 1 | | | 4049 |
| U15,16 | 7 | 14 | | | 4011 |
| U18 | 1 | | | 2 | 79M05 |
| U19 | 18 | 4 | 3 | | 3861A |
| U20 | 8 | 16 | | | 4585 |
| U21,25 | 7 | 14 | | | 4066 |
| U23 | 8 | 16 | | | 4094 |
| U24 | 8 | 16 | | | 4014 |

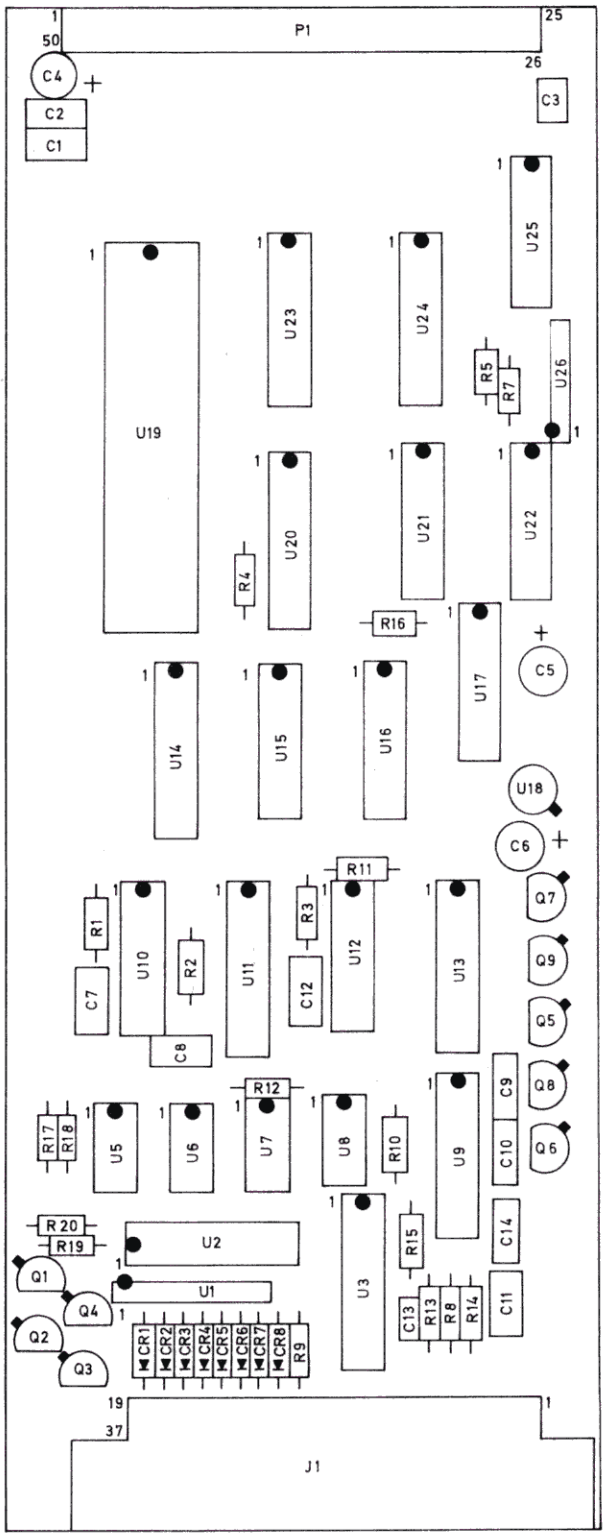
NOTES :-

± 20% D.C. VOLTAGES MEASURED WITH A 20 KΩ/V METER OR EQUIV.

TEST CONDITIONS

SCORE INPUT AT 2400 Bd
OUTPUT CLOCK TIED TO INPUT
CLOCK INPUT WORDS 1,2,5
CONTINUOUSLY FROM
e.g. CA 617

**Circuit: Score Interface Module A6 A1** Fig.App. 2.4




RACAL

| TH3416 | DO8459 |
|---|---|
| 1 | 5 |

Layout : SCORE Interface Board A6A1

Fig. App. 2.5

# APPENDIX 3

## CHANNEL INTERFACE BOARD

## CONTENTS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| 9 | Revertive Channel Data | 2 |
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| 12 | Read Strobe Inputs | 3 |
| 13 | Remote - On Signal | 4 |
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| 16 | BRIEF SOFTWARE DESCRIPTION | 5 |
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| 20 | REMOTE SWITCH ROUTINE | 6 |
| 21 | CHANNEL INTERFACE ROUTINE | 7 |
| | COMPONENTS LIST | |


## Illustrations


| | Fig. |
|---|---|
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# CHANNEL INTERFACE BOARD

## INTRODUCTION

1. This handbook supplement describes an optional facility comprising a channel interface board with associated microcomputer firmware which may be internally fitted into the RA1792 receiver. It provides an interface for extended control of 100-channel selection with revertive indication and band search or clarifier operation in conjunction with units such as the MA1100 Operator Terminal Unit or the MA1107 Automatic Search Unit.

2. The channel interface board is mounted on the inner face of the receiver right-hand chassis side member and plugs into the microcomputer board (A6A2). Note that since the same location is used to house the optional SCORE interface board, the channel interface board can only be fitted at the expense of the SCORE interface board, and vice versa.

## FACILITIES

3. The channel interface board will except two decades of BCD channel number information (eight lines) to select a channel in the range 00 to 99, and provides a revertive indication using the same format. A Receiver Select Enable Line controls the loading of the new information into the receiver.

4. Frequency sweeping in 10 Hz increments is provided using an UP/DOWN line and a clock input. The maximum receiver frequency sweep rate is 100 kHz per second, which corresponds to a clock frequency of 10 kHz.

5. A clarifier on line is provided to limit the sweep to plus and minus 500 Hz for use as a clarifier control. A tune enable line is used to restore tuning control to the receiver front panel shaft encoder whilst the receiver is set to REMOTE*, and whilst in the remote mode and indication is provided via a Remote On Line.

6. Mode selection is not provided as the required mode for a particular channel is stored in the receiver memory.

## CIRCUIT DESCRIPTION

7. The following circuit description should be read in conjunction with the circuit diagram of the channel interface board given in fig. 1.

### Channel Selection

8. The forward channel select data, in inverted BCD format (i.e. )V for '1' or ON, pulled high internally to +12 V for '0' or OFF), is applied to the data inputs of a pair of tri-state inverting buffers U8 and U4. With a '1' at the output disable (OD) inputs of these devices, all Q outputs enter the tri-state or high-impedance condition to allow common casing of the outputs. When U8 and U4 are output enabled (para. 12), the channel select data is routed to the receiver via resistor package U6 and open-collector output transistors Q10 to Q21.

Revertive Channel Data

9. Revertive channel number information from the receiver is routed, under software control, to the data inputs of two quad D-type latches U12 and U13. With the polarity (POL) inputs of these two devices connected to )V, data is clocked into and latched at the Q outputs of U12 and U13 by a logic '0' level at P1 pin 43 (Port 1(3)). The latched data at the Q outputs is routed to the associated extended control unit via resistor package U11 and open-collector output transistor Q2 to Q9. The revertive channel data is also available when the receiver is set to local control, and may thus be used to display remotely the current channel number.

Control Lines

10. Logic '0' DOWN, TUNE ENABLE, CLARIFIER ON and RECEIVER CHANNEL SELECT ENABLE signals, originated by the associated control unit, are routed to the microcomputer via diodes CR10 to CR13, resistor package U17, inverting buffers U18, resistor package U21 and open-collector output transistors Q15 to Q18. The UP/DOWN line is used for receiver fine tuning purposes, where a 0V input results in the DOWN condition, and an open-circuit input (pull-up to +12 V by U18) results in the UP condition. The receiver frequency is increased or decreased in small steps (usually 10 Hz) at a rate determined by the clock frequency at A6A1J1 pin 23. If the CLARIFIER ON line is also at 0V, then the fine-tuning range is limited to a maximum of plus and minus 500 Hz.

11. The TUNE ENABLE line is specifically provided for the MA1107 Automatic Search Unit. When the TUNE ENABLE switch on the front panel of the MA1107 is held depressed, the 0V TUNE ENABLE signal is produced and the receiver may then be manually tuned even through REMOTE is selected. The last of the four control lines, RECEIVER CHANNEL SELECT ENABLE, has already been mentioned (para. 3) and must be set to '0' for new channel selection data to be accepted by the receiver microcomputer.

Read Strobe Inputs

12. A logic '0' read strobe signal is applied to P1 pin 36 (port 1(0)) or P1 pin 42 (port 1(2)) to read the output data from dual BCD up-counter U20a, U20b, via tri-state non-inverting buffers U5, U9 (para. 14), or channel select data from tri-state inverting buffers U8, U4 respectively. The read strobe input signals are level-shifted from 5V TTL applied to NOR gates G5, G6 and G7. These gates are arranged such that regardless of the state of the input signals applied to G7, the outputs of G5 and G6 can never both be at logic '1', a precaution to prevent both sets of data being applied simultaneously to the same output lines. Thus a '0' at P1 pin 36 results in a '1' at the output of G5, and this is inverted by U18 to remove the output disable condition from buffers U5 and U9. Similarly, a '0' at P1 pin 42 results in a '1' at the output of G6, and this is inverted by U18 to remove the output disable condition from buffers U8 and U4. A logic '0' at the output disable pins of U5 and U9 is also applied to NAND gate G1 to force a '1' at the output and so inhibit the clock signal whilst the counter state is read. A logic '1' at the output of G5 is also applied to monostable U7 which forms part of a remote-on circuit (para. 13).

Remote-On Signal

13. Whilst REMOTE in selected at the receiver, the read counters strobe signal (at P1 pin 36) is pulsed once approximately every five milliseconds. The resulting positive-going pulses at the output of G5 are applied to the re-trigger input of monostable U17 to maintain a '1' at the Q output, and then a '0' at the open-collector output of Q1. When the receiver is set to local control, the re-trigger input is removed, and after the time period set by R2, C1 (approximately 15 milliseconds) the Q output goes to '0' and the logic '0' remote-on signal is removed.

BCD Counters

14. The clock signal at J1 pin 23, which m ay be any frequency up to a maximum of approximately 10 kHz, is applied via CR1, U17 clock disable gates G1, G2, G3 and switch filter R7, C9, U19 to the clock input of dual BCD up-counter U20a, U20b. NAND gate G1 is used to inhibit the clock whilst the read-counters operation is taking place ('0' at U18 pin 2), and NAND gates G2, G3 prevent a false positive-going edge at the clock input of U20 when a '1' is forced at the output of G1. The counter stages are reset either by a logic '0' power-on reset signal at P1 pin 2, or by a logic '0' clear-counters signal from the microcomputer at P1 pin 36. Both of these signals are converted from 5 V levels to 12 V levels by U14, and the presence of either signal results in a '1' at the output of NAND gate G8 to reset both sections of U20.

Power Supplies

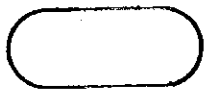
15. The required supplies at +15 V and +12 V are obtained from the receiver via P1 pins 47 and 46 respectively; these supplies are also routed to the external connector A6A1J1 (pins 3 and 21) for connection to external equipment (the MA1107) requires a 12 V supply only).

BRIEF SOFTWARE DESCRIPTION

16. Functional flow diagrams are given for the receiver REMOTE pushbutton routine (fig. 3) and for the channel interface routines (figs. 4 and 5). An explanation of the symbols used in these diagrams is given below.

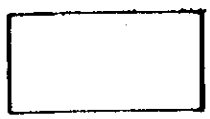
SYMBOLS

17. (1) Entry/Exit



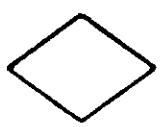
This symbol represents the entry to or the exit from a routine.

(2) Process



This symbol represents any kind of processing function, e.g. to the process of executing a defined operation or group of operations.

(3) Decision



This symbol represents a decision or switching type of operation that determines which of a number of paths is to be followed.

(4) Subroutine Call

This symbol represents a call to a subroutine.

(5) Connector

This symbol represents an exit to or an entry from another part of the flow diagram.

Arrows

18. The normal direction of flow (figs. 3, 4 and 5) is from top-to-bottom, and from left-to-right. Arrows are normally included where the flow is from bottom-to-top and from right-to-left, but they may also be included elsewhere in the interest of clarity.

Paragraph References

19. The numbers adjacent to the symbols on the functional flow diagrams refer to the corresponding descriptive test sub-paragraph numbers.

REMOTE SWITCH ROUTINE (fig. 3)

20. This routine is part of the overall receiver switch routine, and is entered each time the REMOTE pushbutton is pressed.

(1) REMOTE pushbutton pressed. Proceed to routine (2).

(2) If the receiver is already in the REMOTE mode, i.e. if the remote bit is set, proceed to routine (7), otherwise to routine (3).

(3) If TUNE ENABLE is selected, proceed to routine (4), otherwise to routine (5).

(4) Although REMOTE has been selected, TUNE ENABLE was already selected, and local control is thus preserved. The tune enable return flag is set, and control is returned to the calling routine (exit).

(5) The tune enable return flag is cleared. Proceed to routine (6).

(6) The remote bit is set to initiate the selection of the remote mode. Proceed to routine (9).

(7) Since the receiver is already in the remote mode, the REMOTE pushbutton must have been pressed to return the receiver to the local mode, and the tune enable return flag is consequently cleared.

(8) The remote bit is cleared to initiate the selection of the locak mode. Proceed to routine (9).

(9) If local control has been selected, return to the calling routine (exit), otherwise proceed the routine (10).

(10) Remote channel control has been selected; blank the receiver channel display in readiness for the remotely selected channel display. Return control to the calling routine (exit).

CHANNEL INTERFACE ROUTINE (figs. 4 & 5)

21. (1) The control data from the interface, i.e. up/down, tune-enable, clarifier-on and receiver channel select enable, at port 1 bits 4 to 7, is read by the microcomputer and stored. Proceed to routine (2).

(2) The revertive channel number data is applied to port 0 lines 0 to 7, and port 1 bit 3 is pulsed to latch the data.

(3) If the remote status bit is set, proceed to routine (4), otherwise to routine (7).

(4) If TUNE ENABLE is selected ('0' oreviously read from port 1 bit 5) proceed to routine 5, otherwise to routine (11).

(5) Set the tune enable return flag. Proceed to routine (6).

(6) Since TUNE ENABLE is selected, locak control is restored i.e. the remote status is reset. Exit from the channel interface routine.

(7) If TUNE ENABLE is selected, proceed to routine (8), otherwise to routine (9).

(8) Port 1 bit 0 is pulsed to maintain the remote-on signal. Although the remote status bit is not set, TUNE ENABLE is selected, and control from the associated control unit is maintained. Proceed to routine (6).

(9) If the tune enable return flag is set, indicating that TUNE ENABLE was selected the last time selection of REMOTE was attempted, proceed to routine (10), otherwise to routine (6).

(10) The tune enable return flag is cleared. Proceed to routine (11).

(11) The remote status bit is set. Proceed to routine (12).

(12) Port 1 bit 0 is pulsed to maintain the remote-on signal. Proceed to routine (13).

(13) If the receiver channel select enable signal is present ('0' previously read from port 1 bit 7), proceed to routine (15), otherwise to routine (14).

(14) Clear the receiver channel select enabled flag. Proceed to routine (18) on fig. 5 via connector A.

(15) Pulse port 1 bit 2 and read the channel number data from the interface. Proceed to routine (16).

(16) If the channel number from the interface is the same as the current channel number, proceed to routine (17), otherwise to routine 38 on fig. 5, via connector B.

(17) If the receiver channel select enabled flag is set, exit from the channel interface routine, otherwise proceed to routine (38) on fig. 5, via connector B.

(18) Pulse port 1 bit 0 to read and store the sweep count total (read counters). Proceed to routine (19).

(19) Pulse port 1 bit 1 to clear the sweep counter. Proceed to routine (20).

(20) If the sweep count total is equal to zero, indicating no change since the last time through, exit from the interface routine, otherwise proceed to routine (21).

(21) If CLARIFIER ON is selected ('0' previously read from port 1 bit 6), proceed to routine (25), otherwise to routine (22).

(22) If a '0' was previously rad from port 1 bit 4 (UP selected), proceed to routine (24), otherwise to routine (23).

(23) Clear the clarifier accumulator. Proceed to routine (34).

(24) Clear the clarifier accumulator. Proceed to routine (30).

(25) If a '0' was previously read from port 1 bit 4 (UP selected), proceed to routine (26), otherwise to routine (28).

(26) Add the sweep count total, stored during routine (18), to the clarifier accumulator. Proceed to routine (27).

(27) If the clarifier accumulator is greater than +490 Hz, exit from the interface routine, otherwise proceed to routine (30).

(28) Subtract the sweep count total, stored during routine (18), from the clarifier accumulator. Proceed to routine (29).

(29) If the clarifier accumulator is less than -500 Hz, exit from the interface routine, otherwise proceed to routine (34).

(30) Store the new clarifier acumulator. Proceed to routine (31).

(31) Add the sweep count total, stored during routine (18), to the numerical value of the current working frequency. Proceed to routine 32.

(32) If the result of routine (31) represents a frequency greater than 30 MHz, proceed to routine (33), otherwise to routine (42).

(33) Subtract 30 MHz from the frequency arrived at during routine (31), and store the result for use by routine (43). Proceed to routine (42).

(34) Store the new clarifier accumulator. Proceed to routine (35).

(35) Subtract the sweep count total, stored during routine (18), to the numerical value of the current working frequency. Proceed to routine (36).

(36) If the result of routine (35) represents a frequency less than zero, i.e. a minus quantity, proceed to routine (37), otherwise to routine (42).

(37) Add 30 MHz to the frequency arrived at during routine (35), and store the result for use by routine (43). Proceed to routine (42).

(38) Clear the clarifier accumulator. Proceed to routine (39).

(39) Set the receiver channel select enabled flag. Proceed to routine (40).

(40) Store the new channel number. Proceed to routine (41).

(41) Subroutine LODCHN is called to load the new channel. On completion of the subroutine, proceed to routine (42).

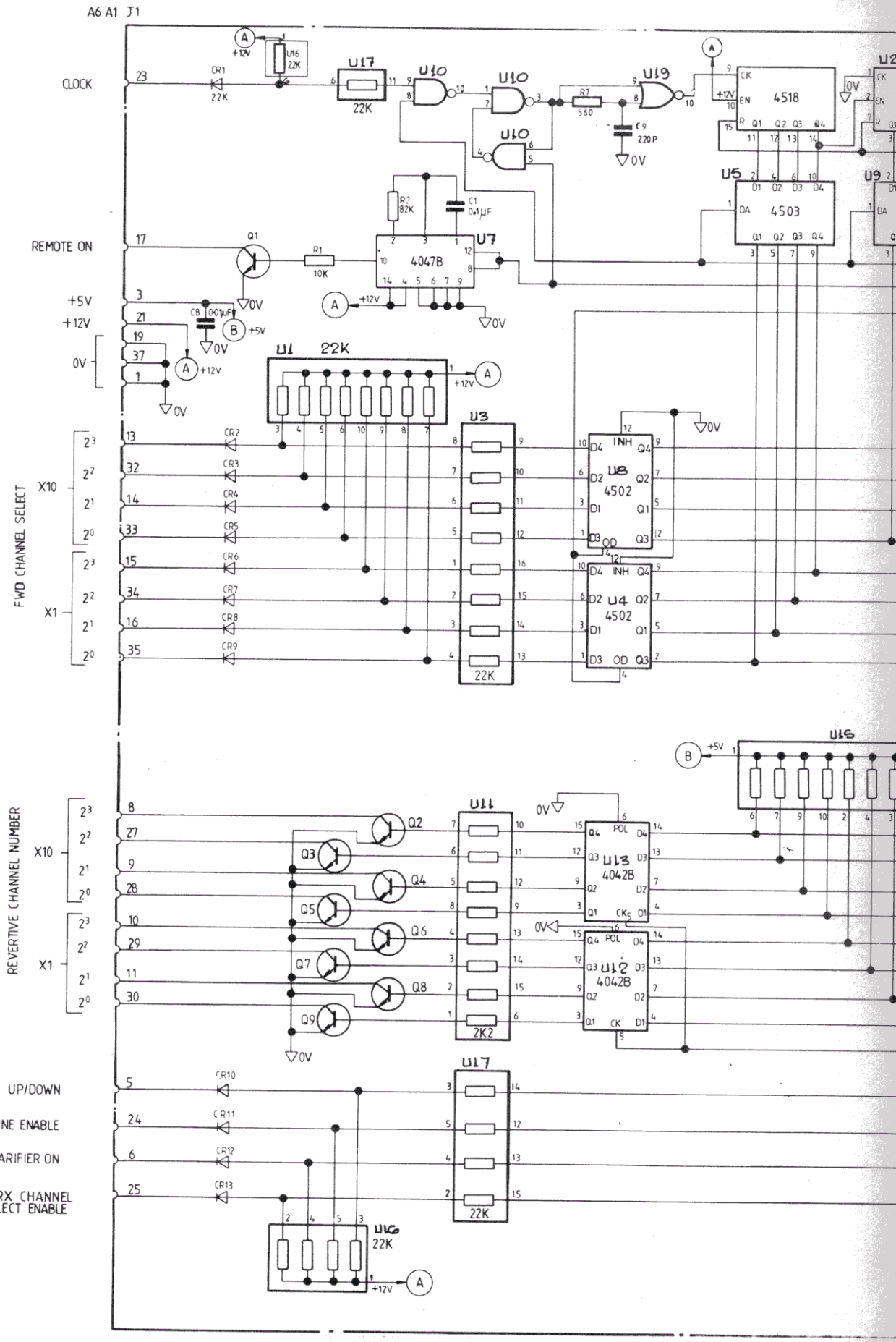
(42) The receiver hardware update bit is set, indicating that various data latches and displays required updating.

(43) Subroutine FRQOUT is called to set up the new receiver frequency. On completion of the subroutine, exit the interface routine.

| Cct. Ref. | Value | Description | Rat. | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| | | **CHANNEL INTERFACE BOARD (ST82455)** | | | |
| **Resistors** | | | | | |
| R1 | 10k | Metal Oxide | | 2 | 914042 |
| R2 | 82k | Metal Oxide | | 2 | 915189 |
| R3 | 22k | Metal Oxide | | 2 | 913493 |
| R4 | 22k | Metal Oxide | | 2 | 913493 |
| R5 | 22k | Metal Oxide | | 2 | 913493 |
| R6 | 22k | Metal Oxide | | 2 | 913493 |
| R7 | 560 | Metal Oxide | | 2 | 917061 |
| **Capacitors** | | | V | | |
| C1 | 0µ1 | Polycarbonate | 100 | 20 +40 | 930801 |
| C2-C8 | 10n | Ceramic Disc | 250 | -20 | 916187 |
| C9 | 220p | Ceramic Disc | 500 | 10 | 931148 |
| **Connectors** | | | | | |
| J1 | | Socket, 37-way | | | 935204 |
| | | Mating plug, 37-way | | | 916507 |
| | | Shell junction, 37-way | | | 918105 |
| | | Retainer, 37-way | | | 914245 |
| P1 | | Plug, PCB, 50-way | | | A07881 |
| **Diode** | | | | | |
| CR1-CR13 | | Silicon IN4149 | | | 914898 |
| **Transistors** | | | | | |
| Q1-Q21 | | NPN Silicon 2N2222A | | | 923217 |
| **Integrated Circuits** | | | | | |
| U1 | 22k | 9 x 22k SIL Resistor Network | | | 935012 |
| U2 | 10k | 9 x 10k SIL Resistor Network | | | 934700 |
| U3 | 22k | 8 x 22k DIL Resistor Network | | | 936375 |
| U4 | | Hex. inverting buffer 4502 | | | 926813 |
| U5 | | Hex. non-inverting biffer 4503 | | | 931004 |

| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| Integrated Circuits (Cont'd) | | | | | |
| U6 | 10k | 8 x 10k DIL Resistor Network | | | 936374 |
| U7 | | Monostable 4047B | | | 930992 |
| U8 | | Hex.inverting buffer 4502 | | | 926813 |
| U9 | | Hex. non-inverting buffer 4503 | | | 931004 |
| U10 | | Quad 2-input HAND gate 4011 | | | 930028 |
| U11 | 2k2 | 8 x 2k2 DIL Resistor Network | | | 932918 |
| U12 | | Quad D-type latch 4042 | | | 930861 |
| U13 | | Quad D-type latch 4042 | | | 930861 |
| U14 | | Quad Level Shifter 40109 | | | 929328 |
| U15 | 22k | 9 x 22k SIL Resistor Network | | | 935012 |
| U16 | 22k | 9 x 22k SIL Resistor Network | | | 935012 |
| U17 | 22k | 8 x 22k DIL Resistor Network | | | 936375 |
| U18 | | Hex. Inverter 4069 | | | 930999 |
| U19 | | Quad 2-input NOR gate 4001 | | | 930027 |
| U20 | | Dual BCD Up-Counter 4518 | | | 931012 |
| U21 | 10k | 8 x 10k DIL Resistor Network | | | 936374 |
| Miscellaneous | | | | | |
| | | 14-PIN DIL IC Socket | | | 930605 |
| | | 16-PIN DIL IC Socket | | | 930606 |

| CCT REF | +5 | +12V | 0V |
|---|---|---|---|
| U4 | — | 16 | 8 |
| U5 | — | 16 | 8 |
| U7 | — | 14 | 7 |
| U8 | — | 16 | 8 |
| U9 | — | 16 | 8 |
| U10 | — | 16 | 8 |
| U12 | 16 | — | 8 |
| U13 | 16 | — | 8 |
| U14 | 1 | 16 | 8 |
| U18 | — | 14 | 7 |
| U19 | — | 14 | 7 |
| U20 | — | 16 | 8 |




MODULES

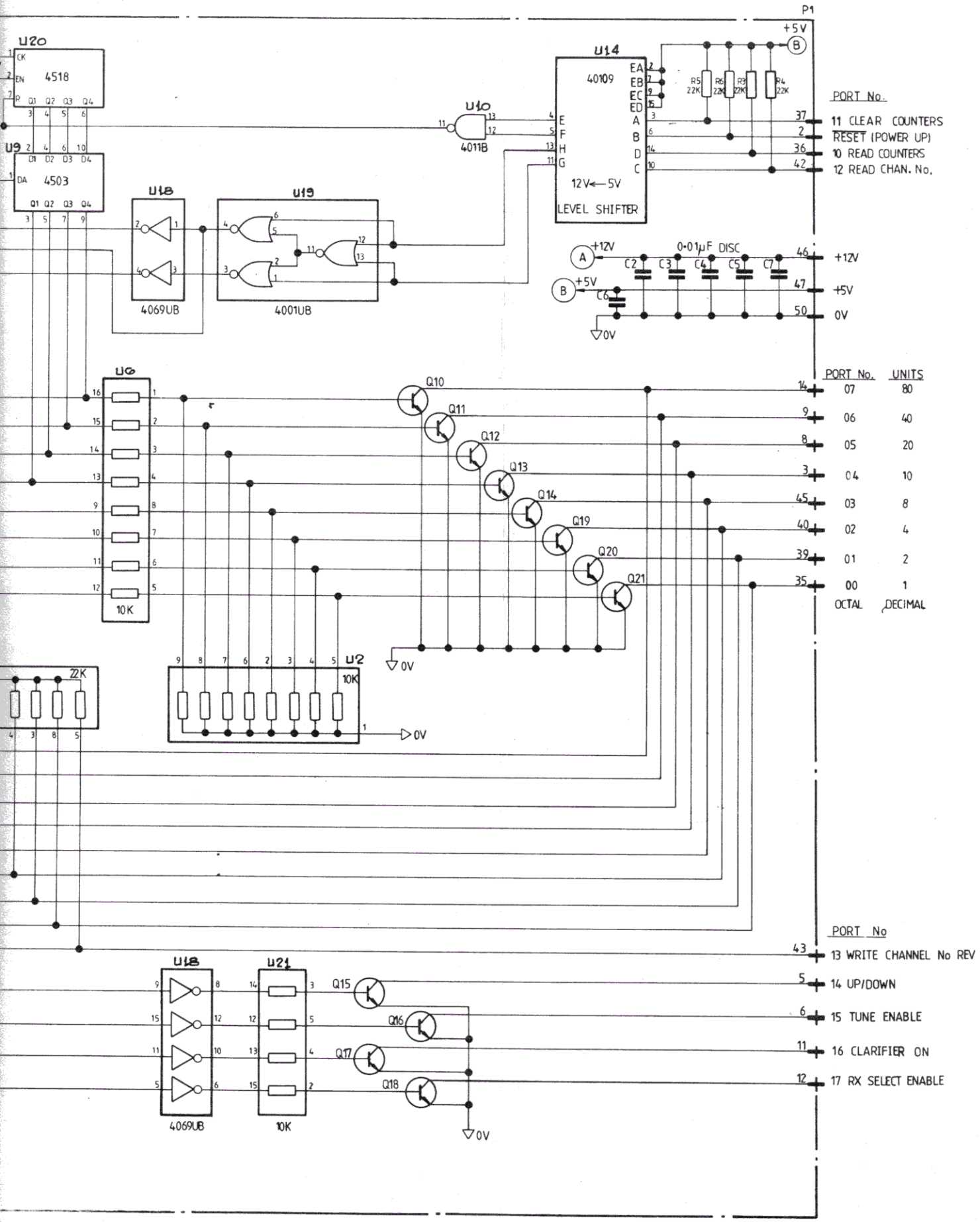
U4, U8 ——— 4502
U5, U9 ——— 4503
U20 ——— 4518
U7 ——— 4047
U10 ——— 4011
U12 U13 ——— 4042
U14 ——— 40109
U18 ——— 4069
U19 ——— 4001

TRANSISTORS
Q1 – Q21 ——— 2N2222A

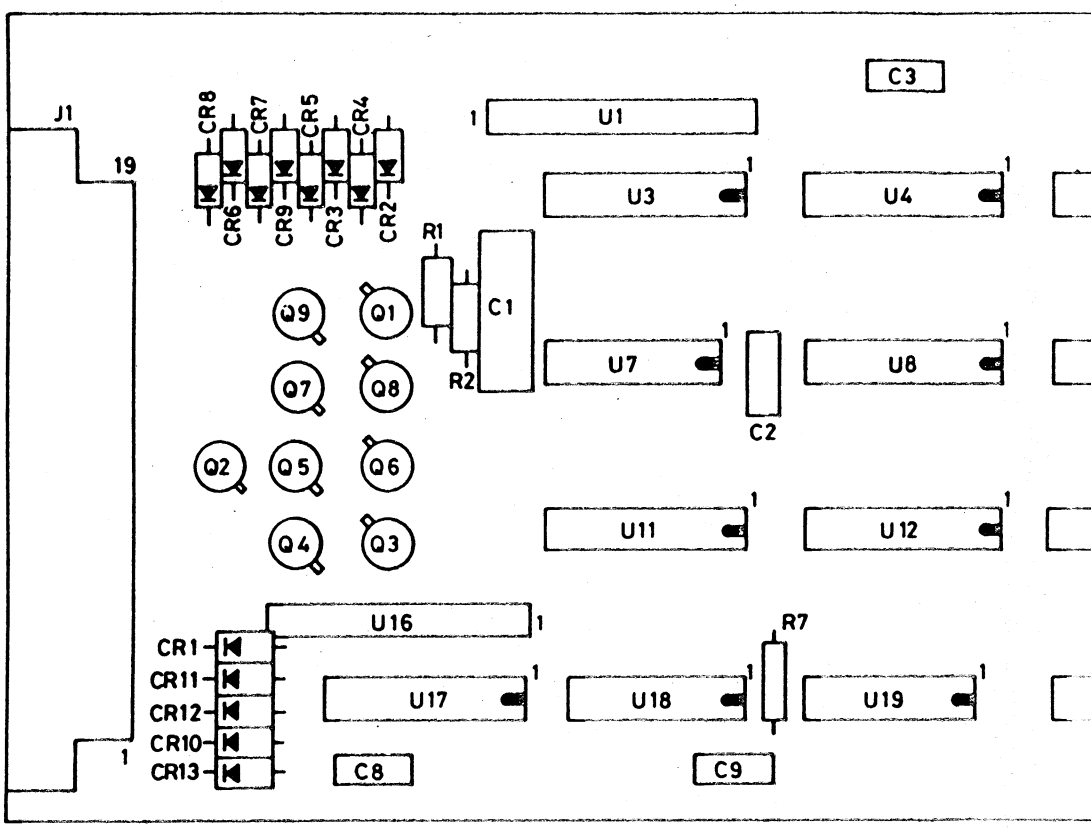
DIODES
D1 – D13 ——— IN4149

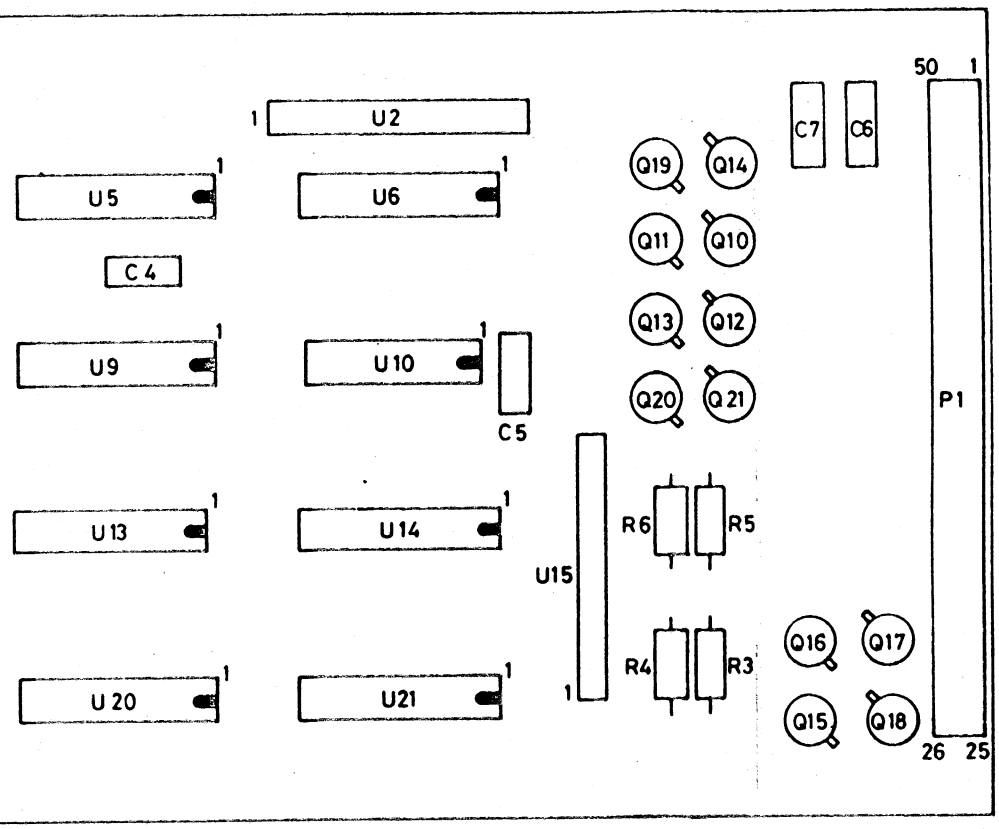
RACAL

| TH3416 | DC82455 |
|---|---|
| 3 | |

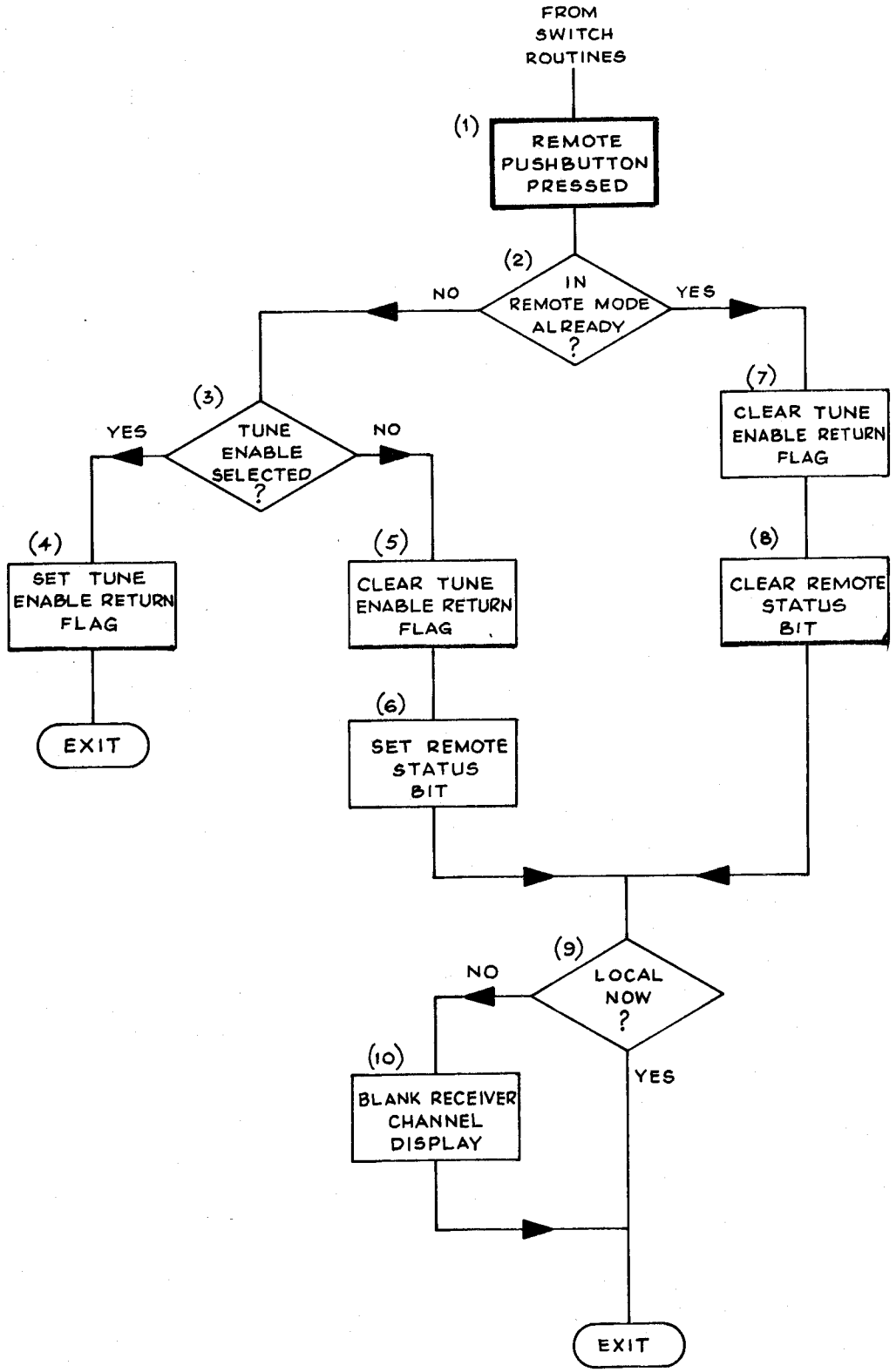



Circuit:
Channel Interface Board App.3 Fig.1


J1
19
1
CR8
CR7
CR5
CR4
CR6
CR9
CR3
CR2
R1
R2
C1
C2
C3
U1
U3
U4
U7
U8
U11
U12
U16
U17
U18
U19
R7
C8
C9
Q9
Q1
Q7
Q8
Q2
Q5
Q6
Q4
Q3
CR1
CR11
CR12
CR10
CR13




Layout:
Channel Interface Board App.3 Fig.2

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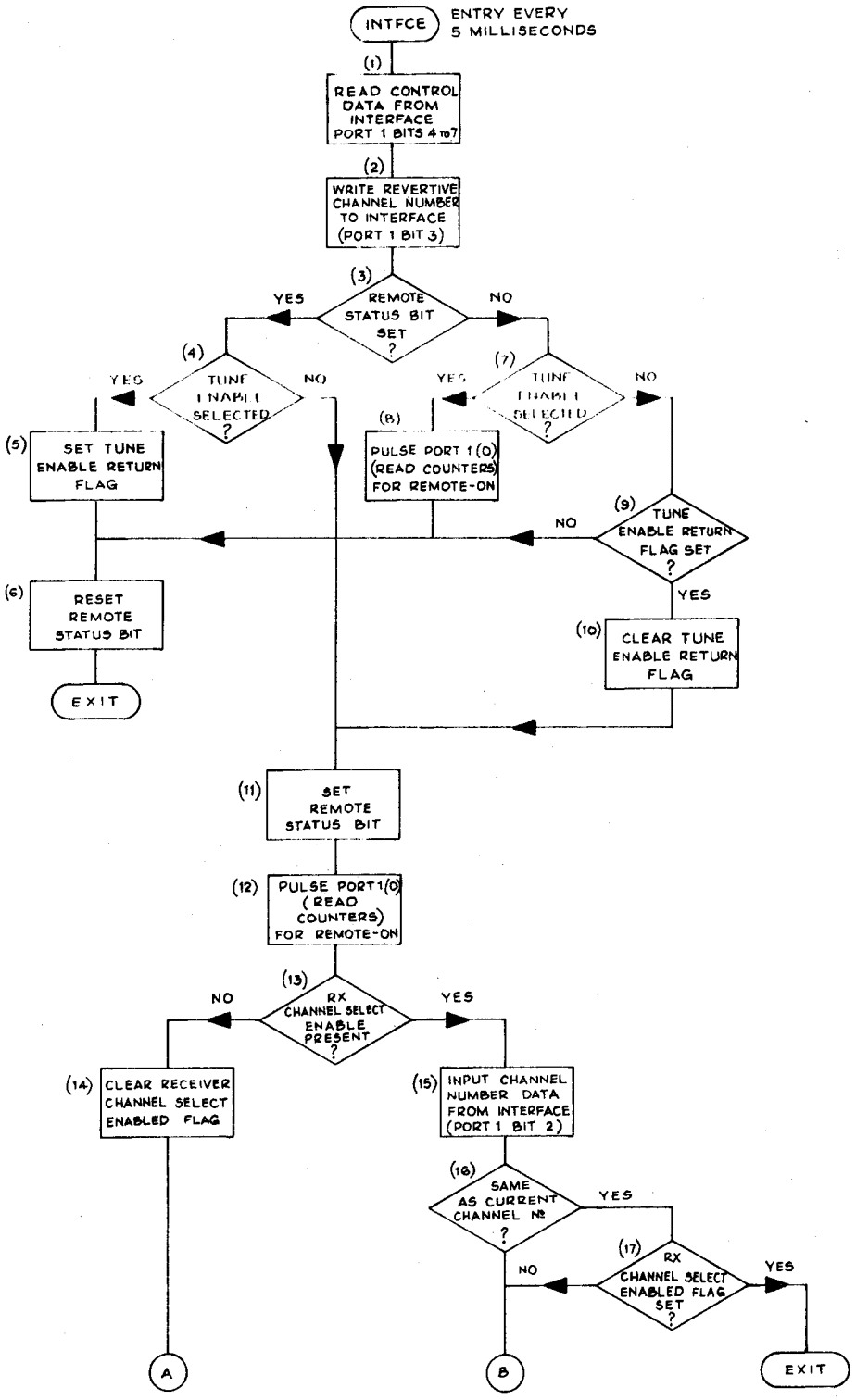
TH3416

REMOTE Switch Routine App.3 Fig.3

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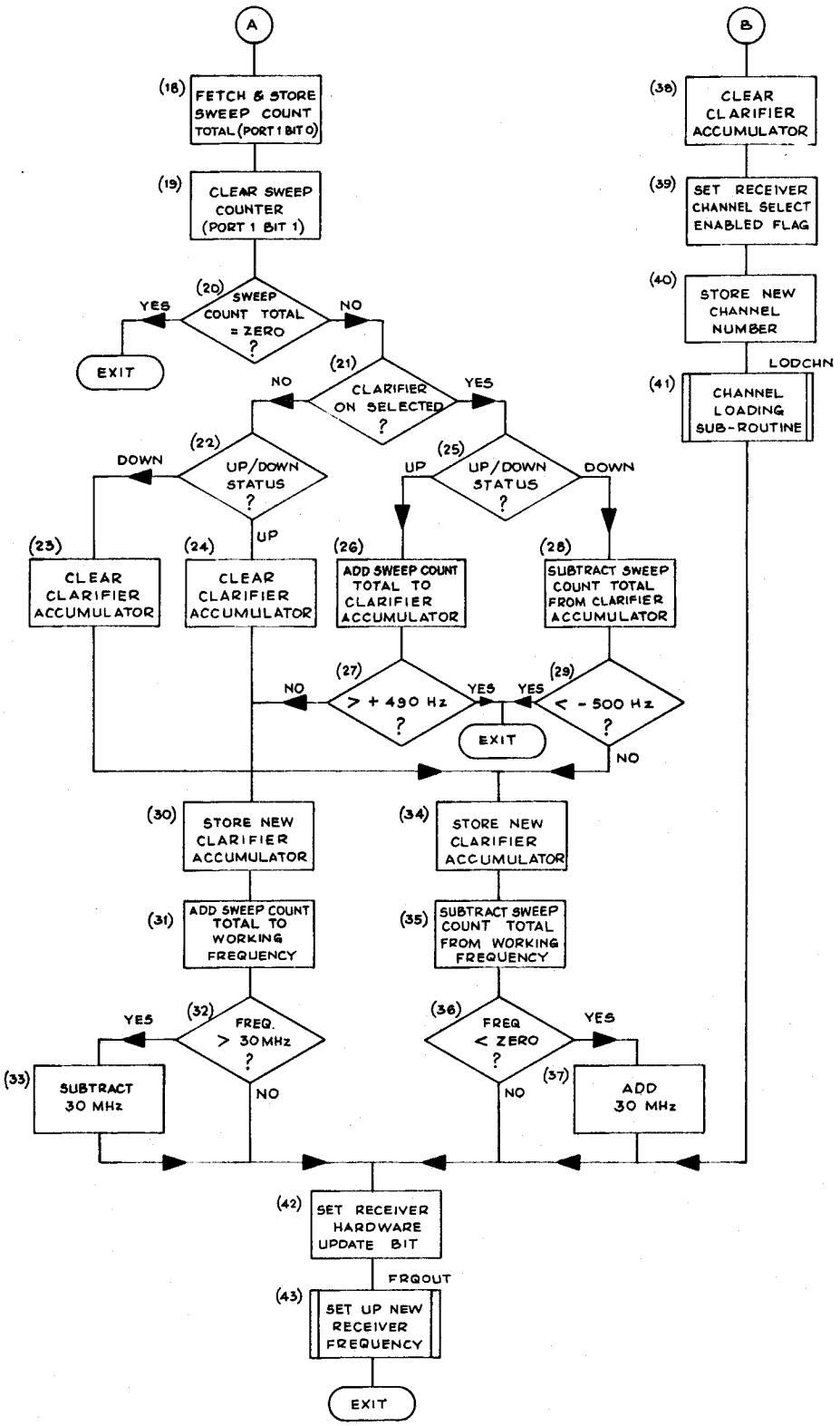
**Interface Routine (Sheet 1)** App. 3 Fig. 4

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TH3416

Interface Routine (Sheet 2) App. 3 Fig. 5

# APPENDIX 4

# IEEE 488 REMOTE CONTROL OPTION

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## ILLUSTRATIONS


| Fig. No. | |
|---|---|
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| App. 4.2 | IEEE-488 Remote Control Interface: Circuit |

# APPENDIX 4

## IEEE 488 REMOTE CONTROL OPTION

### INTRODUCTION

1. This Appendix contains information concerning the IEEE-488 bus system remote control option available for the RA 1792 receiver. This option enables controllable functions of the RA 1792 receiver to be programmed and monitored by any suitable controller which can be interfaced to the standard IEEE-488 bus.

2. Paras. 10 to 28 contain information on the operation of this option, paras. 29 to 57 contain details of the interface between the RA 1792 receiver and the IEEE-488 bus system.

### FUNCTIONAL DESCRIPTION

3. Each controllable function of the RA 1792 receiver can be programmed via the IEEE-488 bus system by sending the appropriate command character (the details of which are given in para. 11), followed by a valid parameter indicating the new value required for that function.

4. There is no command to set the receiver to remote. However, the interface is responsive to the Remote Local interface function, the complete capability being supported. That is, the receiver may be set to remote by the controller to receive a command.

### PARTS COMPLEMENT

#### General

5. There are currently four IEEE 488 kits available although it is possible other kits will become available with time. This is due to the fact that receiver operational software and the IEEE 488 software is combined. Any change to receiver operational software involves a different IEEE 488 kit even though the IEEE 488 conditions are unchanged.

#### Description

6. Four kits are available for the following receiver operational conditions.

i) 10 Hz steps GA filters (i.e. offset 3 KHz)
ii) 1 Hz steps GA filters (i.e. offset 3 KHz)
iii) 10 Hz steps GB filters (i.e. normal 3 KHz)
iv) 1 Hz steps GB filters (i.e. normal 3 KHz)

GA filters are 300 Hz, 1 KHz, 3.2 kHz*, 6 KHz, 16 KHz, USB (3.2 KHz), LSB (3.2 KHz)

* The 3.2 KHz is derived by the use of the USB filter and an IF shift of 1.7 KHz.

GB filters: 300 Hz, 1 KHz, 3.2 KHz*, 6 KHz, 16 KHz, USB (3.2 KHz), (USB (3.2 KHz), LSB (3.2 KHz).

* This filter is physically fitted and no IF shift applies.

Kit Complement

7. Each kit comprises the following items:-

a) i) EPROMS P85060
ii) Interface Board 59-0867 (ST 85435)
iii) Supplementary Handbook.

b) i) EPROMS P85061
ii) Interface Board 59-0867 (ST 85435)
iii) Supplementary Handbook.

c) i) EPROMS P85062
ii) Interface Board 59-0867 (ST 85435)
iii) Supplementary Handbook.

d) i) EPROMS P85063
ii) Interface Board 59-0867 (ST 85435)
iii) Supplementary Handbook.

FITTING INSTRUCTIONS

Parts Required

8. (a) IEEE (A6A1) PCB Assembly 59-0867 (ST85435)
(b) Set of EPROMS (2 off)

Fitting Procedure

9. (a) Remove the power lead and the top cover from the RA 1792. Also remove the rear panel blanking plate (part No. B08345), by unscrewing the top fixing screws.

(b) Remove the three screws holding the micro-computer board (A6A2), to the space on the inside of the RA 1792. Lift out the A6A2 board from the guide rails being careful not to short circuit the battery on the A6A2 board.

(c) Plug the IEEE board (A6A1) into the A6A2 board via the edge connector, J1.

(d) Place the combined A6A2/A6A1 assembly back into the guide rails of the RA 1792 and replace the screws which hold the A6A2 board in position. Use three of the screws provided to secure the A6A1 board to the remaining three pillars on the side of the RA 1792.

(e) Secure the back panel mounting plate (part No. B07983), to the rear panel of the RA 1792 such that the switch, S1, Faces outwards.

(f) Finally, the two EPROMS on the A6A2 board must be checked for compatibility, and changed if necessary.

(g) Table 1 gives a cross reference between the receiver options and the associated EPROMS required (Note other options may become available in the future).

(h) If the EPROM needs to be changed, carefully remove the existing device and replace with the correct device.

(j) The two EPROMS are located in the U8 and U9 positions on the A6A2 board.

(k) This completes the installation of the IEEE option for the RA 1792. A functional check may be made using the users external controller as described elsewhere in this supplement.

TABLE 1

RA 1792 OPTION AND EPROM CROSS REFERENCE

| Description | EPROM Drg. Nos. | Fitting Position on A6A2 |
|---|---|---|
| 10 Hz tuning steps, and offset 3 KHz filter. | P85060/1<br>P85060/2 | U8<br>U9 |
| 1 Hz tuning steps, and offset 3 KHz filter. | P85061/1<br>P85061/2 | U8<br>U9 |
| 10 Hz tuning steps, and normalised filters. | P85062/1<br>P85062 | U8<br>U9 |
| 1 Hz tuning steps, and normalised filters. | P85063/1<br>P85063/2 | U8<br>U9 |

## OPERATION

### Equipment Address

10. The RA 1792 receiver has 5 DIP switches on the I/O interface board, which are used to set the equipment address within the IEEE-488 bus system. The allowable addresses and the corresponding switch positions are given in Table 2.

NOTE: The five switches are located adjacent to the rear panel socket. The three DIL switches located on the board, must be set to OFF.

### Programming

11. Command Format After being successfully addressed via the IEEE-488 bus, the receiver will respond to data messages that conform to the rules given below.

(1) All characters must be in ASCII code (see TABLE 3).

(2) All transmitted strings must be terminated by a "Carriage Return" and a "Linefeed" ASCII character (i.e. ØD, ØA in hexadecimal).

(3) The transmitted string must be made up from one or more of the following commands, with an appropriate parameter for each command letter.

Listener Commands

12.

| Command Letter | | Function |
|---|---|---|
| addressable functions | F | frequency in MHz |
| | D | detector |
| | I | IF BW selected |
| | M | AGC mode |
| | B | BFO frequency in KHz |
| | A | IF Attenuation |
| | X | Remote BITE test number |

13. It is not necessary to send all receiver information every time. By using the alphabetic command letter and following this with the new information, any one of the six addressable functions can be changed without disturbing any other.

Frequency e.g. F10.224321, F10.125.

14. The decimal point is optional and there can be up to 2 digits before the decimal point and up to 6 digits after the decimal point, (i.e. 1 Hz tuning steps).

15. CARRIER or VIRTUAL CARRIER, there is no offset for sideband operation.

16. Detector e.g. D3, D4.

| Parameters | Function |
|---|---|
| 1 | AM |
| 2 | FM |
| 3 | CW |
| 4 | ISB |
| 5 | LSB |
| 6 | USB |

IF Bandwidth (Standard filters)

| Parameters | Function |
|---|---|
| 1 | 300 Hz |
| 2 | 1.0 KHz |
| 3 | 3.0 KHz |
| 4 | 6.0 KHz |
| 5 | 16.0 KHz |

When the detector data is set to SIDEBAND, the BFO data and the filter data are ignored. However, any new filter selection or BFO sent during the time the receiver is set to SIDEBAND will be stored and used on the next detector command to CW, AM or FM. The ISB selection of either upper or lower sideband audio at the front panel phone jack is a local only function.

17. AGC Mode e.g. M4, M6

| Parameters | Function |
|---|---|
| 1 | Short AGC, TC 10-15 ms |
| 2 | Medium AGC, TC 100-200 ms |
| 3 | Long AGC, TC 1-4s |
| 4 | Manual |
| 5 | Short variable threshold |
| 6 | Medium vairable threshold |
| 7 | Long variable threshold |

18. BFO Frequency e.g. B1.80, B-2.95, B0.5

This frequency must be 8.00 and -8.00 KHz. There can be up to 2 digits after the decimal point, (i.e. 10 Hz tuning steps).

19. IF Attenuation e.g. A000, A010, A121

The parameter must be a 3 digit integer (between 0 and 150), which gives the minimum attenuation through the receiver (i.e. 000 gives maximum gain). No adjacent numbers will have gain change greater than 3 dB and the possible values cover the range of the receiver.

20. Remote BITE Test Number e.g. X10, X31

The two digit parameter gives the number of the first BITE test to be performed. The BITE test will be carried out in ascending order starting at the number given; i.e. tests with numbers lower than the number given will not be carried out. If an invalid test number is entered, the tests will start at the next largest valid test number.

21. Refer to Para. 58 for details of the BITE tests.

22. The time taken for all these tests is approximately 80 secs. The results of the tests are passed back to the IEEE controller when the receiver is commanded to enter "TALKER" mode. (See section 23).

23. Talker Request Commands There are two additional commands which ask the receiver to TALK back to the controller.

| Command | Function |
|---|---|
| G | Send back all data in the receiver. |
| T | Return the data for the parameters specified. |

24. On receipt of the G command, the receiver sends back to the controller all the data defined in the receiver, not in the storage. That is to say, if SIDEBAND is in the receiver, no IF bandwidth information will be returned. Similarly, if AGC short is operational, no attenuation data will be returned. Appended to this data stream is the BITE test failed number, this number is preceded by an X (e.g. X20) and it represents a BITE test that the receiver has failed on the last BITE operation. If no tests have failed, then X00 is sent.

25. The T command allows the user to specify the data returned to the controller is subsequent TALKER modes. For example, TDB specifies that upon initiation of the next TALK mode, Detector, BFO and status information will be sent.

26. The 'R' parameter may be used after 'T' to return the RF level (between 0 and 150) after IF filtering.

27. Status data will be appended to all TALKER data messages, this is defined as:-

    0 local control
    1 remote control
    2 local control BITE in progress
    3 remote control BITE in progress

28. All data strings sent by the receiver in TALK mode will be terminated by a "CARRIAGE RETURN" and a "LINEFEED".

## TABLE 2 ADDRESS CODES

| Equipment Address (Hexadecimal) | Address Switches | | | | | Talk Address Character | Listen Address Character |
|---|---|---|---|---|---|---|---|
| | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | | |
| 00 | 0 | 0 | 0 | 0 | 0 | @ | SP |
| 01 | 0 | 0 | 0 | 0 | 1 | A | ! |
| 02 | 0 | 0 | 0 | 1 | 0 | B | " |
| 03 | 0 | 0 | 0 | 1 | 1 | C | # |
| 04 | 0 | 0 | 1 | 0 | 0 | D | $ |
| 05 | 0 | 0 | 1 | 0 | 1 | E | % |
| 06 | 0 | 0 | 1 | 1 | 0 | F | & |
| 07 | 0 | 0 | 1 | 1 | 1 | G | ' |
| 08 | 0 | 1 | 0 | 0 | 0 | H | ( |
| 09 | 0 | 1 | 0 | 0 | 1 | I | ) |
| 0A | 0 | 1 | 0 | 1 | 0 | J | * |
| 0B | 0 | 1 | 0 | 1 | 1 | K | + |
| 0C | 0 | 1 | 1 | 0 | 0 | L | , |
| 0D | 0 | 1 | 1 | 0 | 1 | M | - |
| 0E | 0 | 1 | 1 | 1 | 0 | N | . |
| 0F | 0 | 1 | 1 | 1 | 1 | O | / |
| 10 | 1 | 0 | 0 | 0 | 0 | P | 0 |
| 11 | 1 | 0 | 0 | 0 | 1 | Q | 1 |
| 12 | 1 | 0 | 0 | 1 | 0 | R | 2 |
| 13 | 1 | 0 | 0 | 1 | 1 | S | 3 |
| 14 | 1 | 0 | 1 | 0 | 0 | T | 4 |
| 15 | 1 | 0 | 1 | 0 | 1 | U | 5 |
| 16 | 1 | 0 | 1 | 1 | 0 | V | 6 |
| 17 | 1 | 0 | 1 | 1 | 1 | W | 7 |
| 18 | 1 | 1 | 0 | 0 | 0 | X | 8 |
| 19 | 1 | 1 | 0 | 0 | 1 | Y | 9 |
| 1A | 1 | 1 | 0 | 1 | 0 | Z | : |
| 1B | 1 | 1 | 0 | 1 | 1 | [ | ; |
| 1C | 1 | 1 | 1 | 0 | 0 | \ | < |
| 1D | 1 | 1 | 1 | 0 | 1 | ] | = |
| 1E | 1 | 1 | 1 | 1 | 0 | ^ | > |

NOTE: '0' = SWITCH OFF
'1' = SWITCH ON

## TABLE 3 ASCII CHARACTER CODES

| ASCII CHARACTER | OCTAL CODE | DECIMAL CODE | ASCII CHARACTER | OCTAL CODE | DECIMAL CODE |
|---|---|---|---|---|---|
| NUL | 00 | 0 | ( | 50 | 40 |
| SOH | 01 | 1 | ) | 51 | 41 |
| STX | 02 | 2 | * | 52 | 42 |
| ETX | 03 | 3 | + | 53 | 43 |
| ETO | 04 | 4 | , | 54 | 44 |
| ENQ | 05 | 5 | - | 55 | 45 |
| ACK | 06 | 6 | . | 56 | 46 |
| BEL | 07 | 7 | / | 57 | 47 |
| BS | 10 | 8 | 0 | 60 | 48 |
| HT | 11 | 9 | 1 | 61 | 49 |
| LF | 12 | 10 | 2 | 62 | 50 |
| VT | 13 | 11 | 3 | 63 | 51 |
| FF | 14 | 12 | 4 | 64 | 52 |
| CR | 15 | 13 | 5 | 65 | 53 |
| SO | 16 | 14 | 6 | 66 | 54 |
| SI | 17 | 15 | 7 | 67 | 55 |
| DLE | 20 | 16 | 8 | 70 | 56 |
| DC1 | 21 | 17 | 9 | 71 | 57 |
| DC2 | 22 | 18 | : | 72 | 58 |
| DC3 | 23 | 19 | ; | 73 | 59 |
| DC4 | 24 | 20 | < | 74 | 60 |
| NAK | 25 | 21 | = | 75 | 61 |
| SYN | 26 | 22 | > | 76 | 62 |
| ETB | 27 | 23 | ? | 77 | 63 |
| CAN | 30 | 24 | @ | 100 | 64 |
| EM | 31 | 25 | A | 101 | 65 |
| SUB | 32 | 26 | B | 102 | 66 |
| ESC | 33 | 27 | C | 103 | 67 |
| FS | 34 | 28 | D | 104 | 68 |
| GS | 35 | 29 | E | 105 | 69 |
| RS | 36 | 30 | F | 106 | 70 |
| US | 37 | 31 | G | 107 | 71 |
| SP | 40 | 32 | (Apost.) | 140 | 96 |
| ! | 41 | 33 | a | 141 | 97 |
| " | 42 | 34 | b | 142 | 98 |
| # | 43 | 35 | c | 143 | 99 |
| S | 44 | 36 | d | 144 | 100 |
| % | 45 | 37 | e | 145 | 101 |
| & | 46 | 38 | f | 146 | 102 |
| ' | 47 | 39 | g | 147 | 103 |

TABLE 3 ASCII CHARACTER CODES (Continued)

| ASCII CHARACTER | OCTAL CODE | DECIMAL CODE | ASCII CHARACTER | OCTAL CODE | DECIMAL CODE |
|---|---|---|---|---|---|
| H | 110 | 72 | h | 150 | 104 |
| I | 111 | 73 | i | 151 | 105 |
| J | 112 | 74 | j | 152 | 106 |
| K | 113 | 75 | k | 153 | 107 |
| L | 114 | 76 | l | 154 | 108 |
| M | 115 | 77 | m | 155 | 109 |
| N | 116 | 78 | n | 156 | 110 |
| O | 117 | 79 | o | 157 | 111 |
| P | 120 | 80 | p | 160 | 112 |
| Q | 121 | 81 | q | 161 | 113 |
| R | 122 | 82 | r | 162 | 114 |
| S | 123 | 83 | S | 163 | 115 |
| T | 124 | 84 | t | 164 | 116 |
| U | 125 | 85 | u | 165 | 117 |
| V | 126 | 86 | v | 166 | 118 |
| W | 127 | 87 | w | 167 | 119 |
| X | 130 | 88 | x | 170 | 120 |
| Y | 131 | 89 | y | 171 | 121 |
| Z | 132 | 90 | z | 172 | 122 |
| [ | 133 | 91 | { | 173 | 123 |
| \ | 134 | 92 | : | 174 | 124 |
| ] | 135 | 93 | } | 175 | 125 |
| ^ | 136 | 94 | ~ | 176 | 126 |
| _ | 137 | 95 | DEL | 177 | 127 |

## INTERFACE ADAPTOR

29. The following paragraphs describe the operation of the IEEE-488 interface adaptor used in the RA 1792 Receiver. The optional remote control interface (module A6A1) described in the basic receiver manual is a serial interface. The RA 1792 receiver is designed to operate with the serial interface, a parallel interface, the IEEE-488 interface described in this chapter or with no remote control capability.

30. Paragraph 32 to 34 contain general information, paragraphs 35 to 37 contain installation operation data, paragraphs 38 and on contain the theory of operation.

31. This chapter does not contain detailed information on the IEEE-488 bus. Reference should be made to IEEE-STD-488-1975 Digital Interface for Programmable Instrumentation. Copies of this standard are available from IEEE, 345 East 47th Street, New York, NY 10017, or from the American National Standards Institute, 1430 Broadway, New York, NY 10018.

### Functional Description

32. The RA 1792 Receiver equipped with the IEE-488 interface module (A6A1) can function as either a talker supplying status information to the controller, or as a listener, accepting commands from the controller. The controller selects a particular receiver on the bus through a 5 bit address, programmed on each receiver with a 5-pole switch on the rear panel. The receiver address is also used to command the receiver to the talker or listener mode. Para. 37 describes the receiver address switch programming for each mode.

33. The system controller, typically a HPIB calculator or "smart" terminal equipped with an IEEE interface can command the receiver to change any operating parameter in the same manner as the front panel controls. Connection between the receiver and the IEEE bus are made through a separate rear panel connector (A6A1J2). The data transfer between the bus and the receiver is a standard bit-parallel, byte-serial format. There are 16 primary signal leads between the bus and the receiver. These include 8 data lines (D101 through D108), three handshake lines (DAV, NDAC and NRDF) and five bus management lines used to specify how the information on the data lines is to be interpreted.

34. The circuitry on the A6A1 card is used primarily as an interface between the bus and the microprocessor module (A6A2). The circuitry may be divided into three major groups: the bus driver receiver circuits, the General Purpose Interface Adaptor circuit and the micro-processor circuit. The General Purpose Interface Adaptor, or GPIA, is an LSI chip (Motorola MC68488) that accepts the data from the bus and applies it to the microprocessor. The interrupt circuitry permits the microprocessor to stop its current operation, service the controller commands, and then return to its original operation.

### Installation/Operation

35. The following paragraphs contain detailed information on the interface requirements between the RA 1792 receiver and the IEEE-488 bus and general information on command word formating between the controller and the receiver.

Interface Requirements

36. All interface connections between the receiver and the IEEE-488 bus are made through rear panel connector A6A1J2. Table 4 lists the pin number/signal designation for this connector. An Amphenol or Chinch series 57 connector should be used to mate with A6A1J2.

Receiver Address

37. Each receiver on the bus must be assigned a particular address. This is accomplished through the miniature switch (A6A1A1S1) located on the A6A1 module and accessible from the rear of the receiver. Table 2 lists the receiver switch positions and the corresponding addresses that the controller must use to access the receiver as a talker or a listener.

Command Word Format

38. Communications between the controller and the receiver is accomplished through a string of data words. Each word consists of a letter (indicating the function) and several numbers (identifying the value). Each string of data words must be prefixed with the receiver address for talker or listener function and terminated with carriage return/line feed to indicate the end of the message. Paragraphs 11-28 illustrate typical examples of the command word format.

Command Words for Listener

39. When the controller commands the receiver to function as a listener, the command words may be formated as shown in Paras 11-28 or in a more simplified format. For example, the command F1CRLF will cause the receiver to tune to 1 MHz without changing any other operating parameter. The command F20.5 D2 CRLF will cause the receiver to tune to 20.5 MHz in the FM mode. It should be noted that the controller needs to command only the parameters that are to be changed.

40. If an invalid command is received (for example, specifying an operating parameter that is not compatible with te selected mode) the mode command will be implemented while the operating parameter will be held but not used until the proper mode is selected. For example, the command D5 I3 CRLF would command the receiver to the ISB mode with the bandwidth 3 IF filter. The receiver would switch to the ISB mode with its associated filter. The next time the receiver was switched to the AM, FM, or CW mode it would automatically switch to the bandwidth 3 IF filter: unless, of course, the mode command included a different filter command. In a similar manner, the command D4B+1.80 CRLF would command the receiver to the fixed mode with the BFO set to zero. The next time the receiver is set to the CW Variable mode, the BFO will automatically be set to +1.80 KHz.

41. The receiver is also capable of accepting listener commands from the controller while in the local mode (receiver under front panel control). The receiver will store the commands from the controller and automatically implement them when the receiver is switched to the remote mode.

Command Words for Talker

42. The controller can request status information from any receiver on the bus by addressing the receiver as a talker and specifying the type of status data required. As given in para. 23 the letter G in the command word from the controller will cause the receiver to respond with a complete status update. As previously mentioned, the controller commands to the receiver as a listener may be either in the full format or in a simplified format. With the receiver operating as a talker, however, the full format will always be supplied by the receiver. That is, the frequency data will consist of the sign. 2 digits to the left of the decimal point and 6 digits to the right of the decimal point. The detector, bandwidth, AGC mode, and the status words will consist of a sign and 1 digit: the attenuation word will consist of a sign and 2 digits: and the BFO frequency word will consist of a sign. 1 digit to the left of the decimal point and 2 digits to the right.

43. The receiver will also block any "illogical" status data. That is, if the receiver is in the CW fixed mode no BFO data will be supplied; in the ISB. USB. or LSB modes no IF bandwidth filter data will be given: and in the AGC Long, Medium, or Short modes no IF Attenuation data will be given.

44. The controller can also command the receiver to supply only selected data. As shown in para. 23, the letter T in the command word followed by the letters of the designed parameters will cause the receiver to respond only to those parameters. Any invalid requests, (such as requesting BFO data in the CW fixed mode, IF bandwidth data in the sideband mode, or IF attenuation data in a fixed AGC mode) will cause the receiver to respond only with the applicable data. For example, the receiver will respond that it is in the CW fixed mode and not supply any BFO data.

45. A status bit, indicating whether the receiver is in local or remote control, is always supplied as the last status word.

TABLE 4 INTERFACE CONNECTIONS FOR A6A1J2

| PIN NUMBER | SIGNAL DESIGNATION | PIN NUMBER | SIGNAL DESIGNATION |
|---|---|---|---|
| 1 | D101 | 13 | D105 |
| 2 | D102 | 14 | D106 |
| 3 | D103 | 15 | D107 |
| 4 | D104 | 16 | D108 |
| 5 | E01 | 17 | REN |
| 6 | DAV (See Note 1) | 18 | Signal Ground for DAV |
| 7 | NRFD | 19 | Signal Ground for NRFD |
| 8 | NDAC | 20 | Signal Ground for NDAC |
| 9 | IFC | 21 | Signal Ground for IFC |
| 10 | SRQ | 22 | Signal Ground for SRQ |
| 11 | ATN | 23 | Signal Ground for ATN |
| 12 | SHIELD (See Note 2) | 24 | Signal Ground |

NOTE 1:- Pins 6 through 11 should be wired using twisted pair with the second wire in the pair connected to the corresponding signal ground (pins 18 through 23).

NOTE 2:- The Shield Ground at pin 12 should be grounded only at the controller.

THEORY OF OPERATION

46. General The IEEE-488 interface module (A6A1) consists of circuitry comprising the address switch, the IEEE-488 bus transceivers, the general purpose interface adaptor (GP1A) and the microprocessor interrupt circuitry. The address switch sets the receiver address. Transceivers provide compatible bidirectional connections to the IEEE-488 bus. The GPIA, under control of the microprocessor, transmits data bidirectionally between the IEEE-488 bus (through the transceivers) and the microprocessor. Also, the GPIA initiates an interrupt request upon receipt of the receiver address from the controller. The interrupt circuitry requests the interruption of the microprocessor processing and directs the microprocessor to an interrupt vector address for a specific interrupt routine. Figure 4.2 is a schematic of the IEEE-488 module interface.

47. Bus Transceivers The sixteen IEEE-488 bus lines from the controller come into the module through connector J2 and go into four quad transceiver U8, U12, U4 and U1 (MC3448A). Signal flow direction through each line in the transceivers is determined by its SR input. This input is controlled by the T/R1 or T/R2 output from the GPIA.

48. General Purpose Interface Adaptor (GPIA) The IEEE-488 bus lines, through the transceivers, connect to their corresponding terminals on the GPIA (U2-MC68488). Microprocessor connections are made through connector J1 to the GPIA. These connections include data lines DO-D7, clock 2, read-wite R/W and chip select CS. Initialisation of the GPIA is activated through the RESET line. GPIA operation is controlled through fourteen internal registers which are written to and/or read out by the microprocessor, being addressed through CS, RSO, RS1 and RS2. At initialisation of the microprocessor, the microprocessor sets the appropriate GPIA registers to the start states required for proper system operation. For example, the receiver address, set by the address switch (S1) is read (through the microprocessor at initialisation) into one of these registers.

49. Addressing and Interrupt When the controller sets the ATN line true and sends the receiver address on the data lines DIO1-DIO8, the GPIA recognises this and gives an output on its IRQ terminal. This initiates an interrupt request which is a request to the microprocessor to stop normal processing and to force processing to an interrupt routine which will consider that data being received. The interrupt circuitry not only provides the interrupt request but also provides the microprocessor with the interrupt vector, the programme memory address at which the interrupt routine starts.

50. Pin 14 of U10 is the interrupt request line. When the GPIA IRQ output is true, this interrupt request line is true. If the microprocessor is currently blocking, ignoring interrupt requests, the interrupt control bit (ICB) is high. Under this condition gates U11A and U13A prevent an interrupt request going to the microprocessor. If/ICB is present, then the interrupt requesting is made and/PRI and/INT REQ are asserted. The microprocessor will respond to that request by taking ICB high, blocking the interrupt request, and will begin execution of the interrupt routine. A specific set of RB signals are detected through U10 and related gates U15A and U11D. When these signals are received, gates U11C and U11D enable U6 and U7 to output the interrupt vector on the microprocessor bus.

51. Listener Operation The interface module acts as a listener while waiting to be addressed by the controller and when directed by the microprocessor during a microprocessor routine. During these times the GPIA outputs T/R1 and T/R2 and associates gates U5A and U5B set the transceivers (through their SR inputs) so that the interface accepts controller commands and data from the IEEE-488 bus. Here, data on lines D101-D108 is sent directly through to the GPIA from the controller, and the handshaking line DAV (data available) signal is sent directly through from the controller to the GPIA while handshaking lines NRFD (ready for data) and NDAC (data accepted) signals are sent directly through from the GPIA to the controller.

52. The GPIA acts on the data and/or sends it on to the microprocessor. It also performs required handshaking protocol with the controller as directed by the microprocessor through the GPIA internal registers.

53. Talker Operation The interface module acts as a talker when directed by the microcomputers during a microcomputer routine (sending status data to the controller). When acting as a talker, the GPIA sends an output from its service request (SRQ) terminal through the transceiver (which is hardwired for the outgoing direction only) onto the controller to request that the interface send data to the controller. Also, the GPIA outputs T/R1 and T/R2 set the transceivers so that the interface sends data from the GPIA on to the IEEE-488 bus and thus to the controller. Here, data on lines DIO1-DIO8 is sent directly through from the GPIA to the controller, and the handshaking line DAV signal is sent directly through from the GPIA to the controller while handshaking lines NRFD and NDAC signals are sent directly through from the controller to the GPIA.

54. The GPIA transfers data from the microprocessor to the controller and also performs the required handshaking protocol with the controller as directed by the microprocessor.

55. Bus Management Lines ATN, IFC, REN, SRQ and EOI are the IEEE-488 bus management lines. ATN, IFC and REN have their associated transceivers hardwired for direction of signal flow from the controller to the GPIA only. As indicated earlier, ATN is set true by the controller when it wants to clear lines to send a meassge. IFC is used by the controller to select one of two alternative sources of device programming data local or remote.

56. As indicated previously, SRQ is used by the interface to request sending data from the interface to the controller.

57. EOI is bidirectional, controlled by the GPIA, and is used to indicate the end of a message either to the controller of the interface module.

## BUILT-IN TEST ROUTINES

### Operation

58. The operation of the BITE test routines is described fully in chapter 14 of the RA 1792 Technical Manual. There are, however, certain tests which are unique to the IEEE 488 option and other tests which do not exist in this option. A complete list of BITE tests available in the IEEE 488 option is given in table 6 and the associated failure codes are shown in table 8.

59. The test specific to the IEEE 488 option is test 30 which displays (on the front panel) the equipment address as set up on the rear panel.

60. There is also an additional signature analysis routine selected using SA, a 4-pole switch mounted on the microcomputer board A6A2. This is in addition to the tests described in chapter 14 of the RA 1792 Technical Manual. Details of this test are given below.

IEEE 488 Interface Signature Analysis

61. The tests available via the switches on the microcomputer board are as follows:-

| SA | | | | LED State | | ROUTINE RUNNING |
|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 4 | CR1 | CR2 | |
| OFF | OFF | OFF | OFF | ON | ON | Normal receiver operate |
| ON | OFF | OFF | OFF | Flashing | Flashing | ROM Signatures Analysis |
| OFF | ON | OFF | OFF | ON | Flashing | I/O Exercise |
| ON | ON | OFF | OFF | Flashing | OFF | DAC Ramp Test |
| OFF | OFF | ON | OFF | Alternate | Flashing | IEEE I/F Signature Analysis |
| Any Other | | | | Flashing | ON | Continuous Update Mode |

62. To run the IEEE 488 Interface Signature Analysis routine select the correct switch combination (S1, S2, S4 OFF; S3 ON), ensure that the LED's are flashing alternately, and make the following connections to the microcomputer board with the signature analyser.

CLOCK to TP2 , trigger on negative edge
START to TP11, trigger on negative edge
STOP to TP11, trigger on positive edge
GND to TP14

63. Now check the signatures given in table 6, having disconnected the receiver from any other IEEE 488 equipment.

Table 5: Self Test Routine

| Number | Test details |
|---|---|
| 00 | +5 V power supply line voltage test |
| 01 | +12 V power supply line voltage test |
| 02 | +20 V power supply line voltage test |
| 03 | +15 V power supply line voltage test |
| 04 | -15 V power supply line voltage test |
| 05 | -30 V power supply line voltage test |
| 06 | -12 V power supply line voltage test |
| 07 | Display test: All display segments switched on sequentially and then off at a resonably slow rate. |
| 08 | ROM Sumcheck. |
| 09 | Non-destructive RAM test |
| 10 | Non-destructive EAROM test |
| 11 | Reference oscillator varactor line voltage test |
| 12 | B.F.O varactor line voltage test |
| 13 | 1st L.O. varactor line voltage test<br>1st L.O. synthesiser sweep test in 1 MHz steps<br>1st L.O. synthesiser sweep test in 20 kHz steps |
| 14 | 1st I.F. (A3 Module) AGC line voltage test |
| 15 | BFO sweep test: steps BFO and receiver alternately in 10 Hz, 100 Hz and finally 1 kHz steps giving a series of audio voltages when the receiver and BFO are on the same and different frequencies. |
| 16 | Main I.F. AGC/MGC compatiblity<br><br>Receiver set to 99.999000 MHz (-1 kHz), USB, Short, BFO 0.00 kHz.<br><br>Measures audio level. |
| 17 | Measures AGC voltage. Using the remote manual gain control facility, sets to manual gain and forces the AGC line to the voltage previously measured. Checks that audio level is within ±2 dB of the level measured in test 16. |

| Number | Test details |
|---|---|
| 18 | Increases manual gain voltage by 2.5 V (60 dB)<br><br>No filters selected.<br><br>Checks that audio level is below -2 dBm. |
| 19,20 | ISB IF AGC/MGC compatibility<br><br>These test take place only if an ISB IF/AF module (A5) is fitted.<br><br>Tests 16 and 17 repeated with receiver set to +1 kHz, LSB, Short, BFO 0.00 kHz. |
| 21 | Using the DAC and remote manual gain facility, the gain is adjusted to give an audio level equivalent to -2 dBm on the audio meter scale, with the narrowest filter (FL3) selected. Measures audio level. |
| 22-25 | Repeats 21 for filters FL4, 5, 6 and 7. |
| 26 | Chooses maximum level from tests 21 to 25 and checks that remaining four levels are within 6 dB of the maximum level. Failed test number indicates which filter is faulty.<br><br>If all filers are low then fails test 26. |
| 27 | AM detector test: AM is simulated by using the DAC to vary the remote manual gain voltage.<br><br>Measures audio level. |
| 28 | FM detector test: FM is simulated by swinging 1st local oscillator 5 kHz either side of zero nominal frequency. Measures audio level. |
| 30 | Displays in the frequency display area the IEEE interface address, set up on the rear panel via five DIL switches. The display remains for appoximately 2 seconds and then the receiver returns to BITE continuous update mode. |

## TABLE 6 SIGNATURES - IEEE INTERFACE BOARD

| SIGNAL IDENT | SIGNATURE | J1 | U5 | U13 | U14 | U15 | U2 | U11 | U10 | U9 | U7 | U6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 V | 0000 | 1,50 | 7,8 | 7 | 7 | 7,12 | 1 | 7 | 8 | 7 | 2,4,6, 8,12,14 | 2,4,6,8, 10,12,14,15 |
| + V | UFFP | 47 | 14 | 14 | 9,10,14 | 14 | 20 | 14 | 16 | 14 | 16 | 16 |
| IOC Ø | 45H9 | 25 | | | | | 37 | | | | | |
| IOC 1 | 9207 | 22 | | | | | 38 | | | | | |
| IOC 2 | 13CF | 21 | | | | | 39 | | | | | |
| $\overline{\text{RESET}}$ | UFFP | 2 | | | | | 19 | | | | | |
| $\overline{\text{IO READ}}$ | 522U | 32 | 9 | | | | | | | | | |
| R/W | APP1 | | 10 | | | | 5 | | | | | |
| WRITE | UFFP (F) | 49 | | | 11 | | 6 | | | | | |
| IOC 7 | H8UF | 26 | | | 13 | | | | | | | |
| RBØ | 00C0 | 16 | | | | 5 | | | | | | |
| RB1 | 6F50 | 34 | | | 3 | 3 | | | | | | |
| RB2 | HUAU | 17 | 11 | | | 2 | | | | | | |
| RB3 | H228 | 33 | | | 4 | 4 | | | | | | |
| RB4 | 3671 | 18 | | | 5 | | | 12 | | | | |
| ICB | P034 | 28 | | 8,9 | | | | | | | | |
| /PRI | 8587 | 24 | | 3 | | | | | | | | |
| /INT REQ | 8U6U | 27 | | | | | | | | | 11 | |
| - | 85A5 | | 12 | | 6 | | | | | | | |
| - | 796C | | 13 | | 1,2 | | | | | | | |
| $\overline{\text{CS}}$ | 4CF8 | | | | 12 | | 3 | | | | | |
| - | 84A1 | | | | | 1 | | 13 | | | | |
| - | C38H | | | | | | | 11 | 4 | | | |
| $\overline{\text{IRQ}}$ | HAF9 | | | | | | 40 | | | 5 | | |
| - | 0000 (F) | | | | 8 | | | | 9 | | | |
| - | 27A1 | | | | | 9 | | | 3,5 | | | |
| - | 93H0 | | | | | 10 | | | 7,12 | | | |
| - | 6U1P | | | | | | | 9 | 6 | | 10 | |
| - | F9P8 | | | | | 11 | | | 10 | | | |
| - | 3526 | | | | | | | 8 | 11 | | | |
| - | 8157 | | | 5,6 | | 13 | | | | 6 | | |
| - | 7H99 | | | 4 | | | | | | 8 | | |
| - | 5A38 | | | | | | | 10,5 | | | | |
| - | 2607 | | | | | | | | 13 | 4 | | |
| - | PUFH | | | 2 | | | | | 14 | 9 | | |
| - | 1303 | | | | | | | 1,6 | 15 | | | |
| - | U32A | | | | | | | 4 | | | 1 | 1 |
| $\overline{\text{ICB}}$ | 1FUA | | | 1,10 | | | | 2 | | | | |
| - | 997H | | | | | | | 3 | | | 15 | |
| PBØ | 515U | 15 | | | | | 7 | | | | 3 | |
| PB1 | 3CC1 | 38 | | | | | 8 | | | | 5 | |
| PB2 | 9290 | 41 | | | | | 9 | | | | 7 | |
| PB3 | 08C1 | 44 | | | | | 10 | | | | 9 | |
| PB4 | 89P3 | 4 | | | | | 11 | | | | | 3 |
| PB5 | A63U | 7 | | | | | 12 | | | | | 5 |
| PB6 | HF5F | 10 | | | | | 13 | | | | | 7 |
| PB7 | HC22 | 13 | | | | | 14 | | | | | 9 |
| $\overline{\text{IBØ}}$ | UOHF | | | | | | 36 | | | | | |
| $\overline{\text{IB1}}$ | 1291 | | | | | | 35 | | | | | |
| $\overline{\text{IB2}}$ | 12P5 | | | | | | 34 | | | | | |
| $\overline{\text{IB3}}$ | 5059 | | | | | | 33 | | | | | |
| $\overline{\text{IB4}}$ | CCUP | | | | | | 32 | | | | | |
| $\overline{\text{IB5}}$ | FA54 | | | | | | 31 | | | | | |
| $\overline{\text{IB6}}$ | 30A6 | | | | | | 30 | | | | | |
| $\overline{\text{IB7}}$ | 1H33 | | | | | | 29 | | | | | |

Table 7: Failure Interpretation

| Failed test number | Failure indication |
|---|---|
| 00 | 'H' or 'L' ('high' or 'low') plus voltage being measured shown in frequency display. |
| 01 | |
| 02 | |
| 03 | |
| 04 | |
| 05 | |
| 06 | |
| 07 | Visually note any segments which fail |
| 08 | Faulty sumcheck figure and device number |
| 09 | Faulty device number shown. |
| 10 | Faulty device number shown. |
| 11 | Test number and 'Fault' indicator only |
| 12 | Test number and 'Fault' indicator only |
| 13 | Frequency at which synthesiser goes out of lock. |
| 14 | Test number and 'Fault' indicator only |
| 15 | Synthesiser and BFO frequencies at which failure occurs. |
| 16 | |
| 17 | |
| 18 | Test number and 'Fault' indicator only |
| 19 | |
| 20 | |
| 21 | |
| 22 | |
| 23 | Faulty filter bandwidth in bandwidth display |
| 24 | |
| 25 | |
| 26 | Test number and 'Fault' indicator only. |
| 27 | Test number and 'Fault' indicator only. |
| 28 | |
| 30 | Displays IEEE interface address. |

## PARTS LIST CRT CARD ASSEMBLY

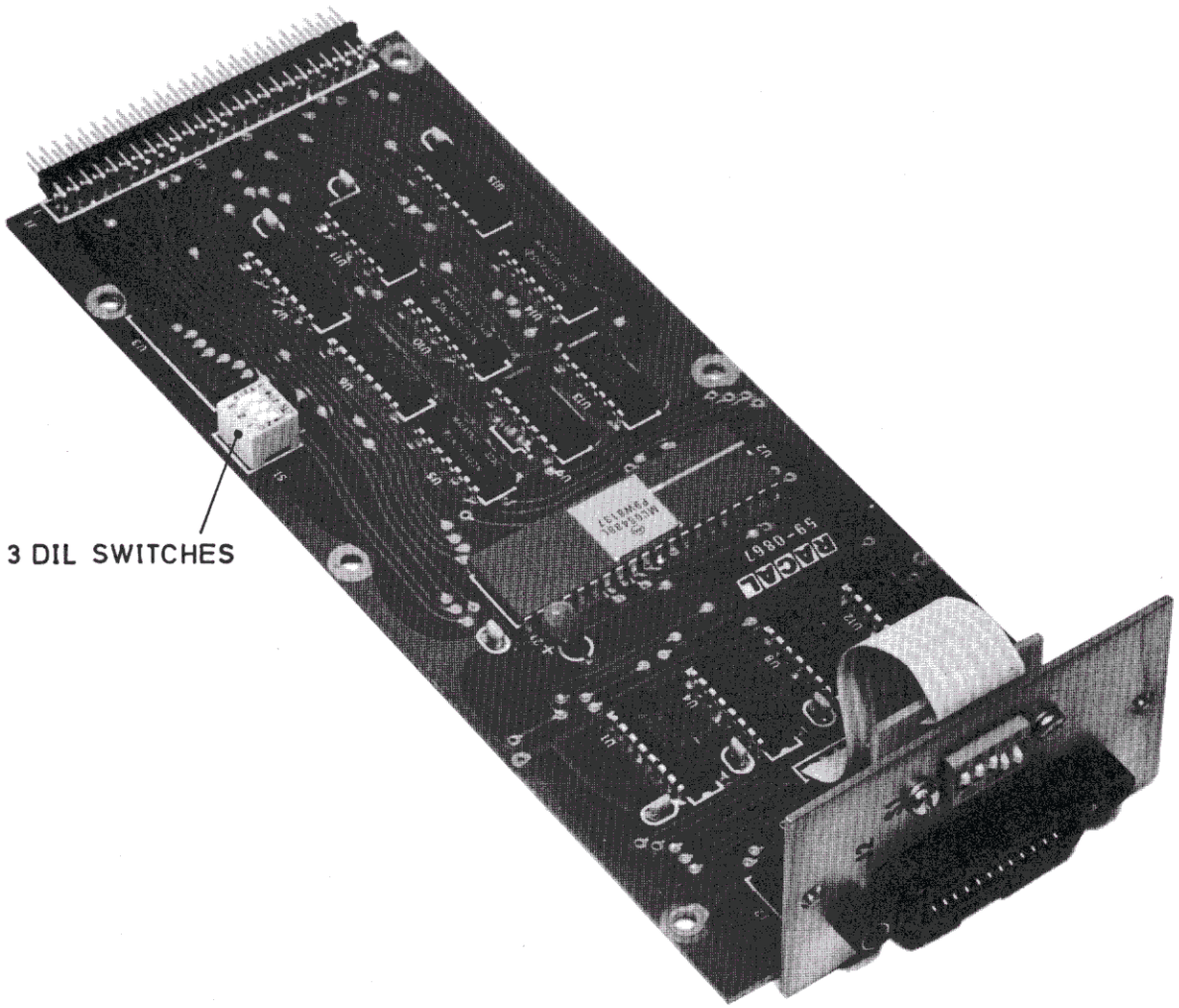
## REMOTE CONTROL INTERFACE (IEEE)

| Reference Designation | Description | RACAL Number | Manufacturer/MIL Part Number |
|---|---|---|---|
| C1,2,3,4,5, 6,7,8. | Capacitor, Ceramic 0.01 mtd ± 20% 50 v. | 21733 | |
| R1 | Resistor, Film, 1K, ± 2% | 12161-102 | |
| U1,U4,U8 U12. | Integrated Circuit (Bus Transceivers) | 36782 | MC3558A |
| U2 | Integrated Circuit (GPIA) (Interface Adapter) | 36783 | MC68488 |
| U3 | Integrated Circuit (Bourns SIP) 10K, 10 pin | 19323-103 | 4310R-101-103 |
| U5 | Integrated Circuit (Quad 2-Input NOR) | 36660 | 74LS02 |
| U6,U7 | Integrated Circuit (Hex 3-State Buffer) | 36694 | 4503 |
| U9 | Integrated Circuit (Dual A-O-1 Gates) | 36781 | 4085 |
| U10 | Integrated Circuit (4 Bit D Flip Flop) | 36675 | 74LS175 |
| U11,U13 | Integrated Circuit (Quad 2-Input NAND) | 36571 | 4011B |
| U14 | Integrated Circuit (Triple 3-Input NAND) | 36633 | 74LS10 |
| U15 | Integrated Circuit (Dual 4-Input NOR) | 36587 | 4002 |
| J1 | Connector, Berg, 50 Pin, 2 Section | A67881 | |
| J2 | Connector AMP | 61255 | Champ No. 552791-4 |
| A6A1A1 | Connector Switch Mounting Plate | B07983 | |
| W1 | Cable Assembly | 55232 | Ansley FSN23B-6 |

## PARTS LIST CRT CARD ASSEMBLY

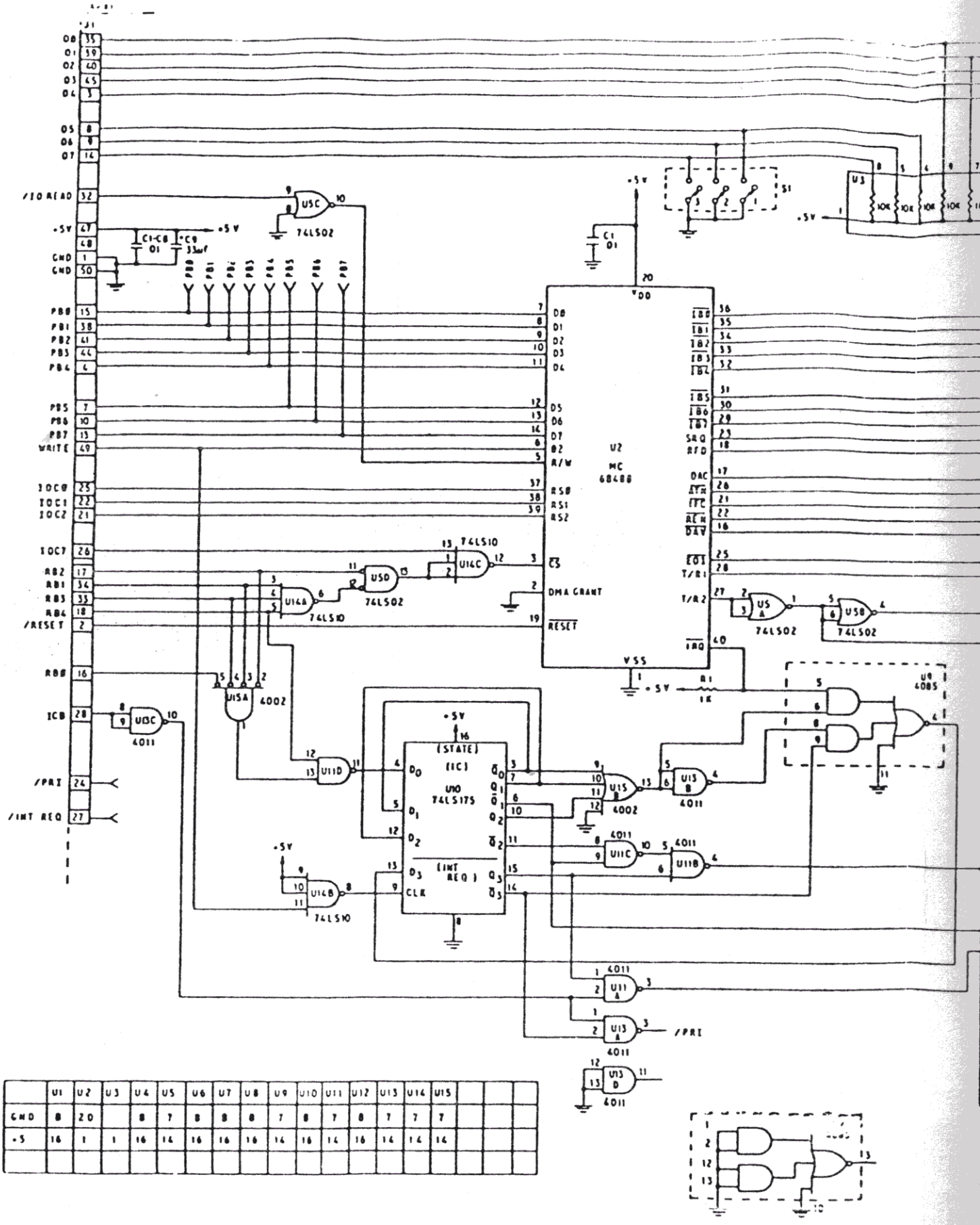
## REMOTE CONTROL INTERFACE (IEEE) (Continued)

| Reference Designation | Description | RACAL Number | Manufacturer/MIL Part Number |
|---|---|---|---|
| J3 | Socket Assembly (Note: 6 socket strip required to mate with W1) | 61253 | Ansley 741 |
| | Assembly, Printed "W" Board | D07975 | |
| | Assembly, CKT Card | D07976 | |
| | Sub Assembly, Switch-A6A1A1S1 W1 Cable PWB (on A6A1A1) | B07984 | |

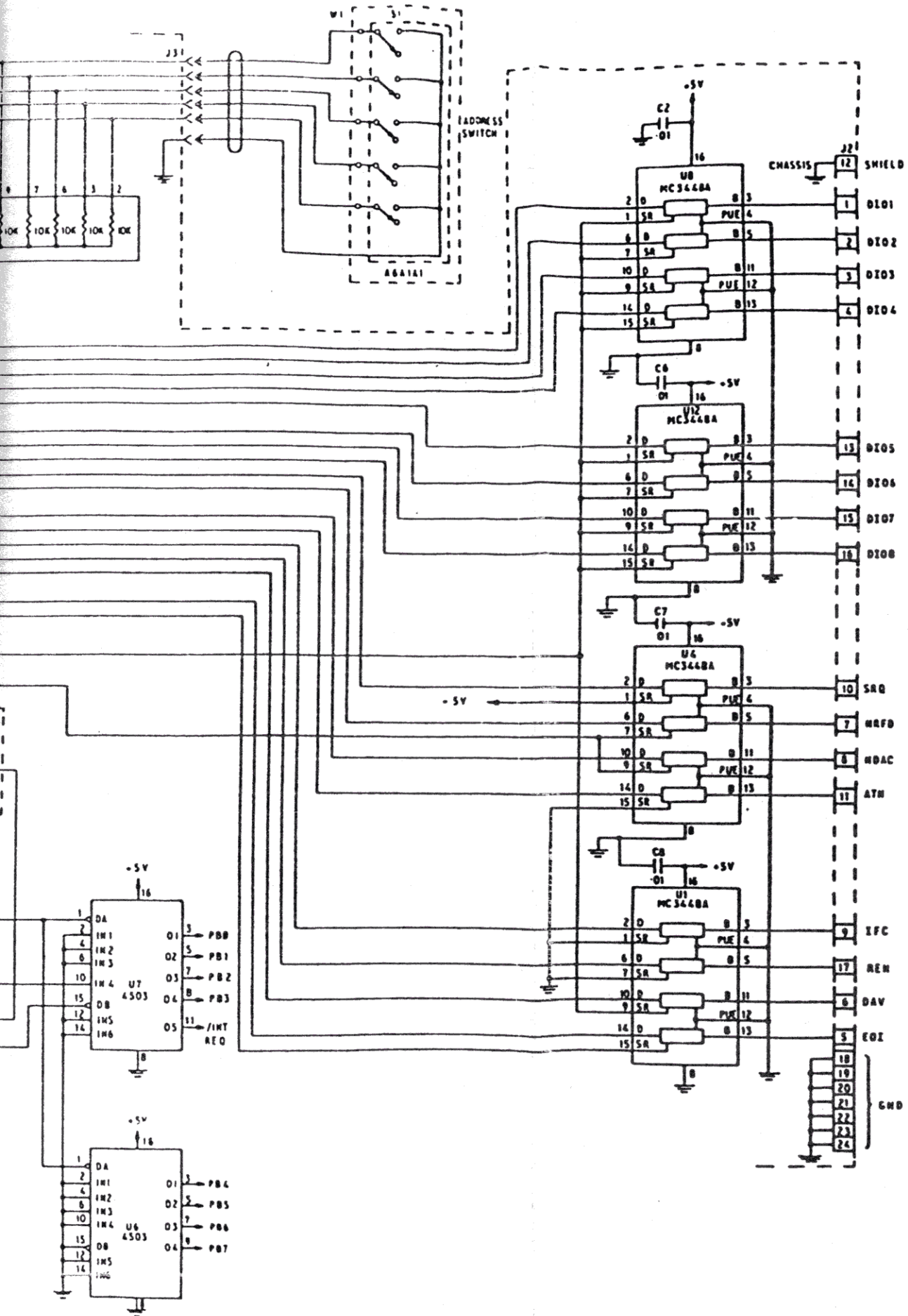



IEEE-488 Interface Module
Type 59-0867 (ST85435)

Fig. App. 4.1




| | U1 | U2 | U3 | U4 | U5 | U6 | U7 | U8 | U9 | U10 | U11 | U12 | U13 | U14 | U15 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | 8 | 20 | | 8 | 7 | 8 | 8 | 8 | 7 | 8 | 7 | 8 | 7 | 7 | 7 | | | |
| +5 | 16 | 1 | 1 | 16 | 14 | 16 | 16 | 16 | 14 | 16 | 14 | 16 | 14 | 14 | 14 | | | |
| | | | | | | | | | | | | | | | | | | |




Remote Control Interface
(IEEE): Circuit

Fig. App. 4.2

# APPENDIX 5

# PANADAPTOR IF MODULE

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| 10. | COMPONENTS LIST | App. 5-2 |


## ILLUSTRATIONS


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| App. 5.1 | Panadaptor IF Module: Circuit Diagram |
| App. 5.2 | Panadaptor IF Module: Component Layout |

# APPENDIX 5

# PANADAPTOR IF MODULE

## INTRODUCTION

1. The Panadaptor IF Module DA 82041 contains an IF amplifier and AGC circuits. The module provides an additional IF output, which is required when using a Signal Display Unit. The Panadaptor is a p.c.b. which plugs into the space in the RA 1792 normally reserved for the ISB board.

## CIRCUIT DESCRIPTION (Fig. App. 5.1)

### Input Amplifier

2. The source impedance of the signal at the input to the board is transformed from 5 kohms to about 200 ohms by Q1 and the signal is then applied to an integrated circuit, gain - controlled amplifier U5. This device contains two amplifier sections, connected in cascade, to provide high gain and AGC range. The input signal is applied via C7 to pin 1 and the output from the first section, at pin 12, is applied, via R18 and C12, to the input of the second section at pin 10. The output taken from pin 7 is applied via a bandpass filter to an emitter follower Q2, and also to the IF output amplifier comprising Q3, Q4, Q5 and from there to the IF OUT jack J2 at a level of 100 mV ±3 dB. The signal is then available at the RA 1792 socket J9.

3. AGC is applied across both sections of U5 via pins 3 and 4, thus providing a control range of approximately 60 dB. The three-terminal regulator U4 serves to stabilize the supply to U5 at 12 volts.

### AGC Detector and Amplifier Stages

4. The IF signal from the emitter follower Q2 feeds the U2 transistor array, connected as a detector. U2B compensates the bias of U2C for temperature changes. The output from U2C feeds the AGC integrator U10A through U1C in series with switch U6D. Switch U6D is controlled by binary coded logic into W1P1 pin 12 (IDB3) through U9. Latch U9 is clocked by the OP3A input to W1P1 pin 24, via Q6. The output from the integrator U10A goes through the AGC filter, which is set for carrier or peak signal AGC through U8D. The filter output goes through stage U10D and on to control the gain of the IF AGC amplifier U5.

5. Three alternate AGC time constants are provided together with AGC 'hang' and 'dump' capabilities. These time constants are selected by the appropriate parallel combination of R29, R30 and R31. R30 and R31 are switched in or out by FET switches U6B and U6C. The switches are controlled by the binary coded logic inputs (through latch U7) on W1P1 pins 5 (IDB6) and 3 (IDB7). U6C ON selects short, U6B ON selects medium and both OFF selects the long time constant. Latch U7 is clocked by the OP3A input to Q1P1 pin 24, via Q6.

6. When selected, the AGC 'hang' circuit disconnects R29, R30 and R31 from the decay circuit by cut-off transistor U2E. This transistor is driven by 'hang' circuit stages U1A and U1B. Capacitor C15 charges, through U1A, when a large encough signal is received from the AGC detector. The voltage on C15, through U1B, cuts off U2E when the signal is removed. This causes the A6C to 'hang' until C15 discharges. Switch U6A, connected across C15, disables the 'hang' circuit when switched to the ON state by the binary coded logic signal from W1P1 pin 8 (IDB8), through U7. Latch U7 is clocked by the OP3A input to W1P1 pin 24.

7. When a 'dump' command is received at U7 pin 1, the Q output of U3A is clocked to a '1', turning on U2D and U8D. This causes the AGC voltage to decay rapidly, until comparator U1A detects a signal at the IF output. This resets U3A and turns off U2D and U8D.

Manual/Remote IF Control

8. When Manual gain is selected, FET switches U8A and U8C are turned ON by the binary coded logic inputs to W1P1 pins 18 (IDBØ) and 16 (IDB2) through latch U9. This allows the IF gain control voltage from the front panel (via W1P1 pin 4) to set the gain through stages U10C and U10A. Latch U9 is clocked by the OP3A input at W1P1 pin 24.

9. The output of the Digital to Analogue Converter (U21 on the Main IF/AF Module A4) is used to control the receiver gain when the receiver is under remote control, by switching on U8B. The DAC voltage is stored by the sample and hold circuit comprising U10C, U8B, R48 and C27 while the DAC is performing the receiver metering functions. When the receiver is under AGC control, the DAC is used to hold the output of U10C at 0 V and also set the AGC voltage on TP8 to 10 V when no signal is present.

COMPONENTS LIST

10. The Panadaptor IF Module DA82041 comprises components as follows:-

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Resistors** | | | | | |
| R1 | 15 k | Resistor Electrosil TR4 | ¼ | 2 | 920645 |
| R2 | 22 k | Resistor Electrosil TR4 | ¼ | 2 | 913493 |
| R3 | 1.5 k | Resistor Electrosil TR4 | ¼ | 2 | 911166 |
| R4 | 100 | Resistor Electrosil TR4 | ¼ | 2 | 910388 |
| R5 | 12 k | Resistor Electrosil TR4 | ¼ | 2 | 917952 |
| R6 | 22 k | Resistor Electrosil TR4 | ¼ | 2 | 913493 |
| R7 | 3.3 k | Resistor Electrosil TR4 | ¼ | 2 | 910111 |
| R8 | 10 k | Resistor Electrosil TR4 | ¼ | 2 | 914042 |
| R9 | 2.7 k | Resistor Electrosil TR4 | ¼ | 2 | 916548 |
| R10 | 560 | Resistor Electrosil TR4 | ¼ | 2 | 917061 |
| R11 | 1 k | Resistor Electrosil TR4 | ¼ | 2 | 913489 |
| R12 | 47 k | Resistor Electrosil TR4 | ¼ | 2 | 913496 |
| R13 | 10 k | Resistor Electrosil TR4 | ¼ | 2 | 914042 |
| R14 | 10 k | Resistor Electrosil TR4 | ¼ | 2 | 914042 |
| R15 | 10 k | Resistor Electrosil TR4 | ¼ | 2 | 914042 |
| R16 | 47 k | Resistor Electrosil TR4 | ¼ | 2 | 913496 |
| R17 | 47 k | Resistor Electrosil TR4 | ¼ | 2 | 913496 |
| R18 | 2 k | Trimmer Electrosil TR4 | ¼ | 2 | 938440 or 916550 |
| R19 | 47 | Resistor Electrosil TR4 | ¼ | 2 | 917063 |
| R20 | 680 | Resistor Electrosil TR4 | ¼ | 2 | 910113 |
| R21 | 1.5 k | Resistor Electrosil TR4 | ¼ | 2 | 911166 |
| R22 | 220 k | Resistor Electrosil TR4 | ¼ | 2 | 921771 |
| R23 | 47 | Resistor Electrosil TR4 | ¼ | 2 | 917063 |
| R24 | 680 | Resistor Electrosil TR4 | ¼ | 2 | 910113 |
| R25 | 50 k | Trimmer Electrosil TR4 | ¼ | 2 | 938441 or 914170 |
| R26 | 22 k | Resistor Electrosil TR4 | ¼ | 2 | 913493 |
| R27 | 4.7 k | Resistor Electrosil TR4 | ¼ | 2 | 913490 |
| R28 | 2.2 k | Resistor Electrosil TR4 | ¼ | 2 | 916546 |
| R29 | 47 k | Resistor Electrosil TR4 | ¼ | 2 | 913496 |
| R30 | 33 k | Resistor Electrosil TR4 | ¼ | 2 | 913495 |
| R31 | 1 k | Resistor Electrosil TR4 | ¼ | 2 | 913489 |
| R32 | 22 k | Resistor Electrosil TR4 | ¼ | 2 | 913493 |
| R33 | 1.5 k | Resistor Electrosil TR4 | ¼ | 2 | 911166 |
| R34 | 10 k | Resistor Electrosil TR4 | ¼ | 2 | 914042 |
| R35 | 10 k | Resistor Electrosil TR4 | ¼ | 2 | 914042 |
| R36 | 1 k | Resistor Electrosil TR4 | ¼ | 2 | 913489 |
| R37 | 1 k | Resistor Electrosil TR4 | ¼ | 2 | 913489 |
| R38 | 15 k | Resistor Electrosil TR4 | ¼ | 2 | 926045 |
| R39 | 47 | Resistor Electrosil TR4 | ¼ | 2 | 917063 |
| R40 | 1 k | Resistor Electrosil TR4 | ¼ | 2 | 913489 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| R41 | 1 k | Resistor Electrosil TR4 | ¼ | 2 | 913489 |
| R42 | 18 k | Resistor Electrosil TR4 | ¼ | 2 | 900994 |
| R43 | 270 k | Resistor Electrosil TR4 | ¼ | 2 | 923598 |
| R44 | 15 k | Resistor Electrosil TR4 | ¼ | 2 | 920645 |
| R45 | 3.3 k | Resistor Electrosil TR4 | ¼ | 2 | 910111 |
| R46 | 1 k | Resistor Electrosil TR4 | ¼ | 2 | 913489 |
| R47 | 22 k | Resistor Electrosil TR4 | ¼ | 2 | 913493 |
| R48 | 10 k | Resistor Electrosil TR4 | ¼ | 2 | 914042 |
| R49 | 1.2 k | Resistor Electrosil TR4 | ¼ | 2 | 911179 |
| R50 | 1 k | Resistor Electrosil TR4 | ¼ | 2 | 913489 |
| R51 | 1 k | Resistor Electrosil TR4 | ¼ | 2 | 913489 |
| R52 | 22 k | Resistor Electrosil TR4 | ¼ | 2 | 913493 |
| R52 | 10 k | Resistor Electrosil TR4 | ¼ | 2 | 914042 |
| R54 | 22 k | Resistor Electrosil TR4 | ¼ | 2 | 913493 |
| R55 | 390 | Resistor Electrosil TR4 | ¼ | 2 | 916331 |
| R56 | 47 k | Resistor Electrosil TR4 | ¼ | 2 | 913496 |
| R57 | 39 | Resistor Electrosil TR4 | ¼ | 2 | 917062 |
| R58 | 100 k | Resistor Electrosil TR4 | ¼ | 2 | 915190 |
| R59 | 10 | Resistor Electrosil TR4 | ¼ | 2 | 920736 |
| R60 | 22 k | Resistor Electrosil TR4 | ¼ | 2 | 913493 |
| R61 | 18 k | Resistor Electrosil TR4 | ¼ | 2 | 900994 |
| R62 | 18 k | Resistor Electrosil TR4 | ¼ | 2 | 900994 |

| Capacitors | | | V | | |
|---|---|---|---|---|---|
| C1 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C2 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C3 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C4 | 1000 pF | Capacitor Ceramic | | 20 | 938408 |
| C5 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C6 | 100 µF | Capacitor Electrolytic | 25 | | 935140 |
| C7 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C8 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C9 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C10 | 0.022 µF | Capacitor Ceramic | | 20 | 930219 |
| C11 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C12 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C13 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C14 | 15 µF | Capacitor Tantalum | 35 | 20 | 922418 |
| C15 | 6.8 µF | Capacitor Tantalum | 20 | 20 | 921179 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| C16 | 0.01 µF | Capacitor Ceramic | 50 | 20 | 938053 |
| C17 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C18 | 1500 pF | Capacitor Mica | 500 | ±1 | 943146 |
| C19 | 33 pF | Capacitor Mica | 400 | ±1p | 902222 |
| C20 | 1500 pF | Capacitor Mica | | | 938435 |
| C21 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C22 | 0.01 µF | Capacitor Ceramic | 50 | 20 | 938053 |
| C23 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C24 | 15 µF | Capacitor Tantalum | 35 | 20 | 922418 |
| C25 | 15 µF | Capacitor Tantalum | 35 | 20 | 922418 |
| C26 | 0.01 µF | Capacitor Ceramic | 50 | 20 | 938053 |
| C27 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C28 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C29 | 6.8 µF | Capacitor Tantalum | 20 | 20 | 921179 |
| C30 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |
| C31 | 470 µF | Capacitor Electrolytic | 25 | | 938439 |
| C32 | 15 µF | Capacitor Tantalum | 35 | 20 | 922418 |
| C33 | 0.1 µF | Capacitor Ceramic | | 20 | 938406 |

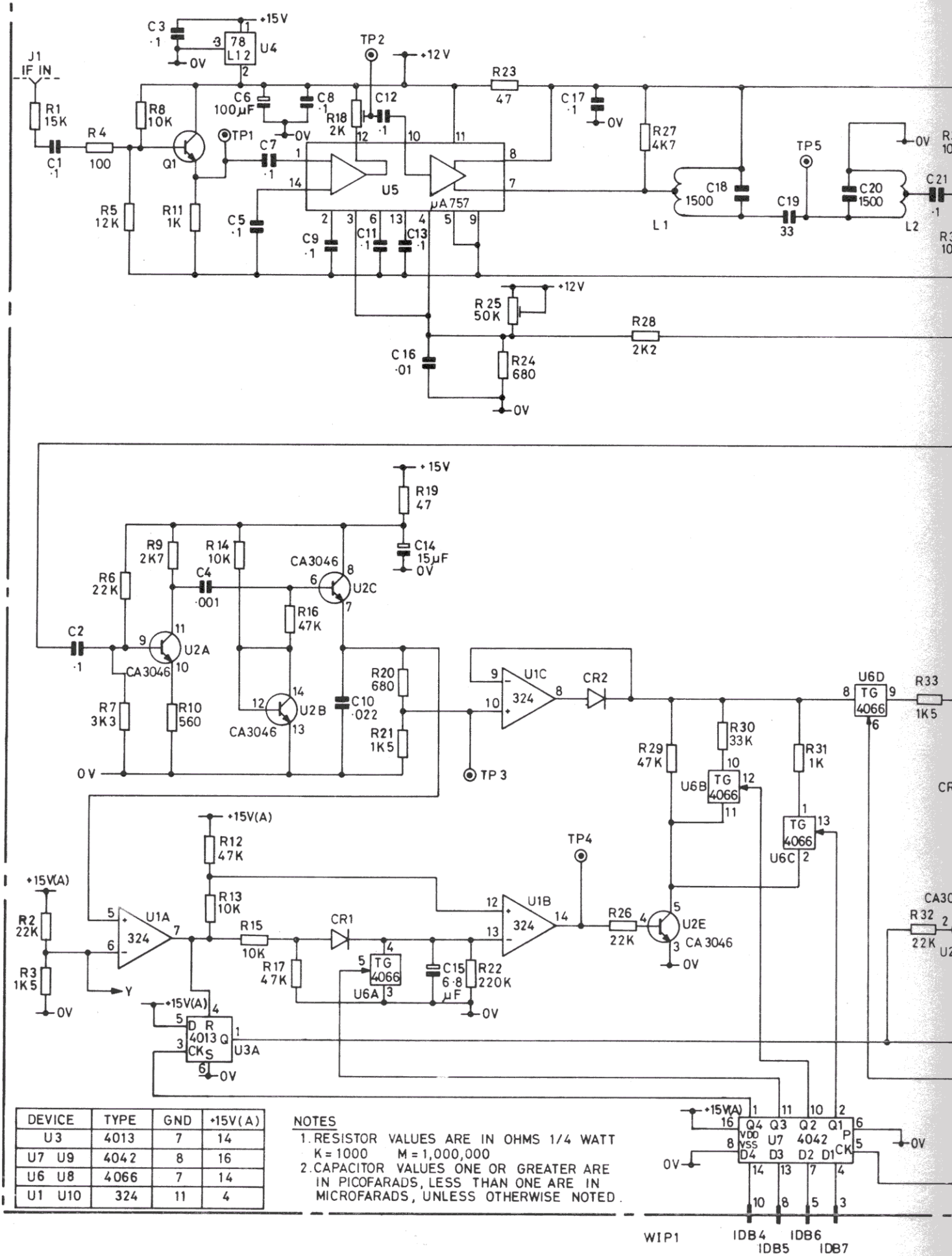
## Diodes

| | | |
|---|---|---|
| CR1 | 1N916 | 913480 |
| CR2 | 1N916 | 913480 |
| CR3 | 1N916 | 913480 |
| CR4 | 1N916 | 913480 |
| CR5 | 1N916 | 913480 |
| CR6 | 1N916 | 913480 |

## Transistors

| | | |
|---|---|---|
| Q1 | 2N5089 | 938417 |
| Q2 | 2N5089 | 938417 |
| Q3 | 2N5089 | 938417 |
| Q4 | 2N5089 | 938417 |
| Q5 | 2N5089 | 938417 |
| Q6 | 2N2369 | 906842 |

| Cct. Ref. | Value | Description | Rat | Tol % | Racal Part Number |
|---|---|---|---|---|---|
| **Integrated Circuits** | | | | | |
| U1 | LM324N | Quad Op. Amp Signetics | | | 925944 |
| U2 | CA 3046 | Transistor Array | | | 922907 |
| U3 | MC1401BCP | Dual 'D' Type Flip Flop | | | 933644 |
| U4 | UA78L12HC | Voltage Regulator | | | 933496 |
| U5 | U6A7757393 | IF Amp | | | 938442 |
| U6 | CD4066BE | Quad Bilateral Switch | | | 930148 |
| U7 | MC14042BCL | Quad Latch | | | 938443 |
| U8 | CD4066BD | Quad Bilateral Switch | | | 930148 |
| U9 | MC14042BCL | Quad Latch | | | 938443 |
| U10 | LM 324N | Quad Op. Amp | | | 925944 |
| **Connectors** | | | | | |
| J1 | | Plug, Coaxial, RF 50 ohms | | | 938429 |
| J2 | | Plug, Coaxial, RF 50 ohms | | | 938429 |
| W1P1 | | Cable Assembly, comprising | | | B08226 |
| | | Connector, PCP, 34-way | | | 938571 |
| | | Cable, PVC Ins, 34-way | | | 927430 |
| | | Socket, 34-way | | | 934213 |
| | | Clamp, strain relief, 34-way | | | 934214 |
| **Inductors** | | | | | |
| L1 | | Coil Assembly | | | AT 82390 |
| L2 | | Coil Assembly | | | AT 82390 |




| DEVICE | TYPE | GND | +15V(A) |
|---|---|---|---|
| U3 | 4013 | 7 | 14 |
| U7 U9 | 4042 | 8 | 16 |
| U6 U8 | 4066 | 7 | 14 |
| U1 U10 | 324 | 11 | 4 |

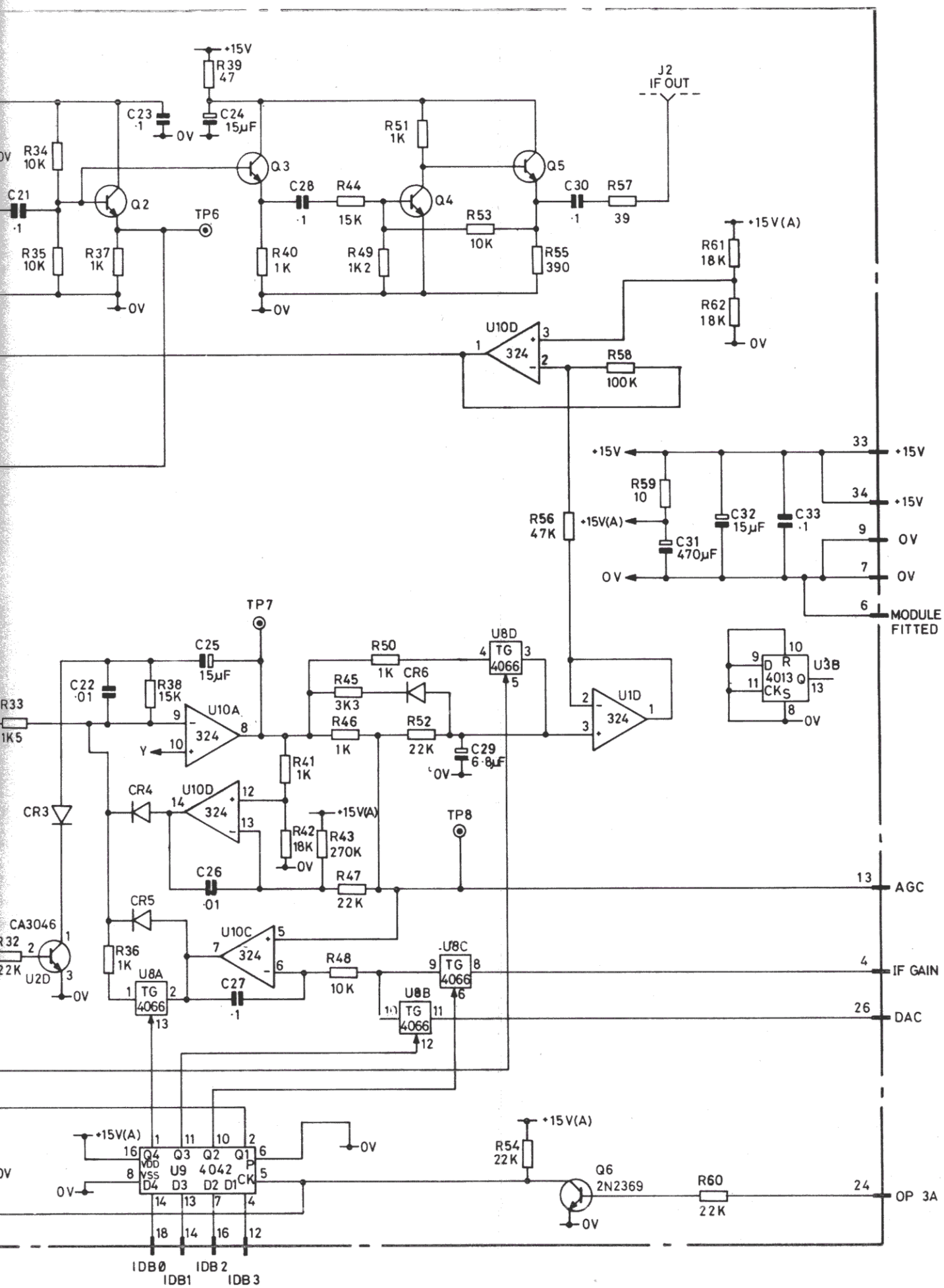
NOTES

1. RESISTOR VALUES ARE IN OHMS 1/4 WATT
   K = 1000 M = 1,000,000
2. CAPACITOR VALUES ONE OR GREATER ARE IN PICOFARADS, LESS THAN ONE ARE IN MICROFARADS, UNLESS OTHERWISE NOTED.

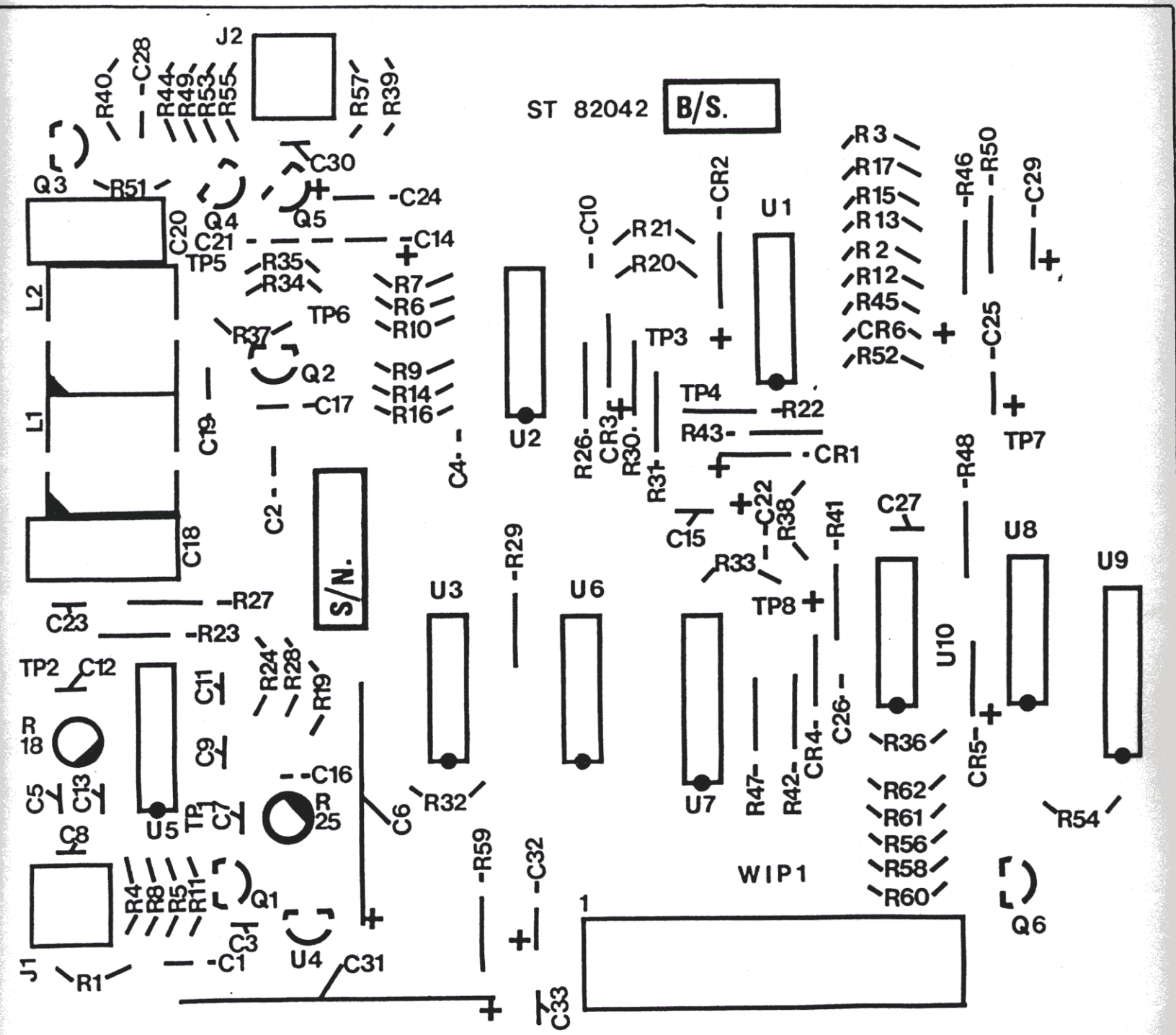
RACAL

TH3416 DC82042

2




**Panadaptor IF Module: Circuit Diagram** Fig. App. 5.1




Panadaptor IF Modu
Layout

# Racal (Slough) Limited

## RA1792 HF COMMUNICATIONS

## RECEIVER

Handbook addendum for receivers fitted with the 100KHz IF output option:

51-3001 Standard option

51-3002 Dual ISB option

**RACAL (SLOUGH) LIMITED**
Duke Street . Windsor . Berks SL4 1SB
Telephone: WINDSOR 69811
Cables/Grams: RACAL WINDSOR
Telex: 847013

RACAL

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| Chapter | Description |
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| | Circuit Diagram No. 49-0123 |
| | Circuit Diagram No. 49-0122 |

# CHAPTER 1

# GENERAL DESCRIPTION

## CONTENTS


Paragraph

1 INTRODUCTION

2 FUNCTIONAL DESCRIPTION

3 SPECIFICATION


## ILLUSTRATIONS


Figure No:

1 Functional Block Diagram

# CHAPTER 1

## GENERAL DESCRIPTION

### 1. INTRODUCTION

This addendum contains information concerning the 100kHz output options available for the RA1792 receiver.

The option is available in two forms:-

51-3001 100kHz IF Output Option

51-3002 100kHz IF Output and ISB IF Output

When fitted these options provide outputs centred at 100kHz to replace the 455kHz of the standard receiver.

The option is available as a modification kit containing all connectors and cables required, and is simple to install.

The kits can only be applied to option receivers which do not have a derived 3kHz filter, ie, the use of the USB filter and a suitable IF offset. The receivers must be fitted with a normal symmetrical filter and have the corresponding software programme incorporated.

Example:-

1. Standard Receiver
   Filter reference GA ie. derived 3kHz filter.
   Programme P80961 (1Hz steps).
   Receiver unsuitable for use with these mod. kits.

2. Option Receiver
   Filter reference GB ie. fitted with 3kHz symmetrical filter Drawing Number 07883-3.
   Programme P80965 (10Hz steps) or P80969 (1Hz steps).

Receiver suitable for use with these mod. kits.

N.B. For advice on this matter, refer to the local RACAL representative.

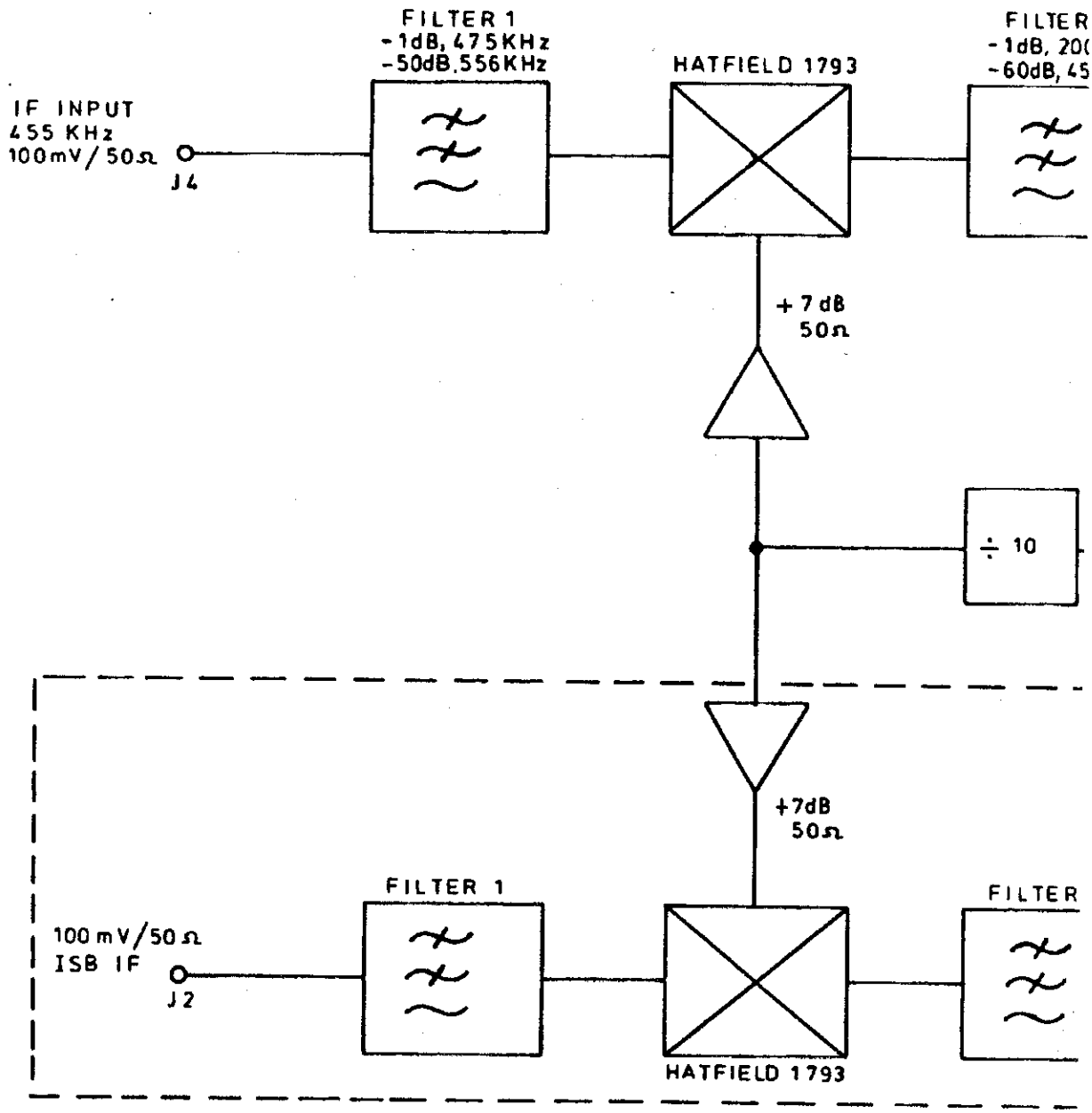
## 2. FUNCTIONAL DESCRIPTION

The 100kHz Option coverts the standard 455kHz receiver 2nd IF to 100kHz, by a single frequency conversion. The local oscillator, at 555kHz, contained within the option module is phase locked to the receiver frequency standard.

The option has unity gain, the nominal output being 100mV into 50Ω.

## 3. SPECIFICATION

| | |
|---|---|
| Input Impedance | 50 ohms |
| Output Impedance | 50 ohms |
| Output Level | 100mV nominal |
| Power Supply | 15 volts DC 200mA |
| Size | 140 x 140 x 40mm |




Admel P/2/036 x A4 SIZE

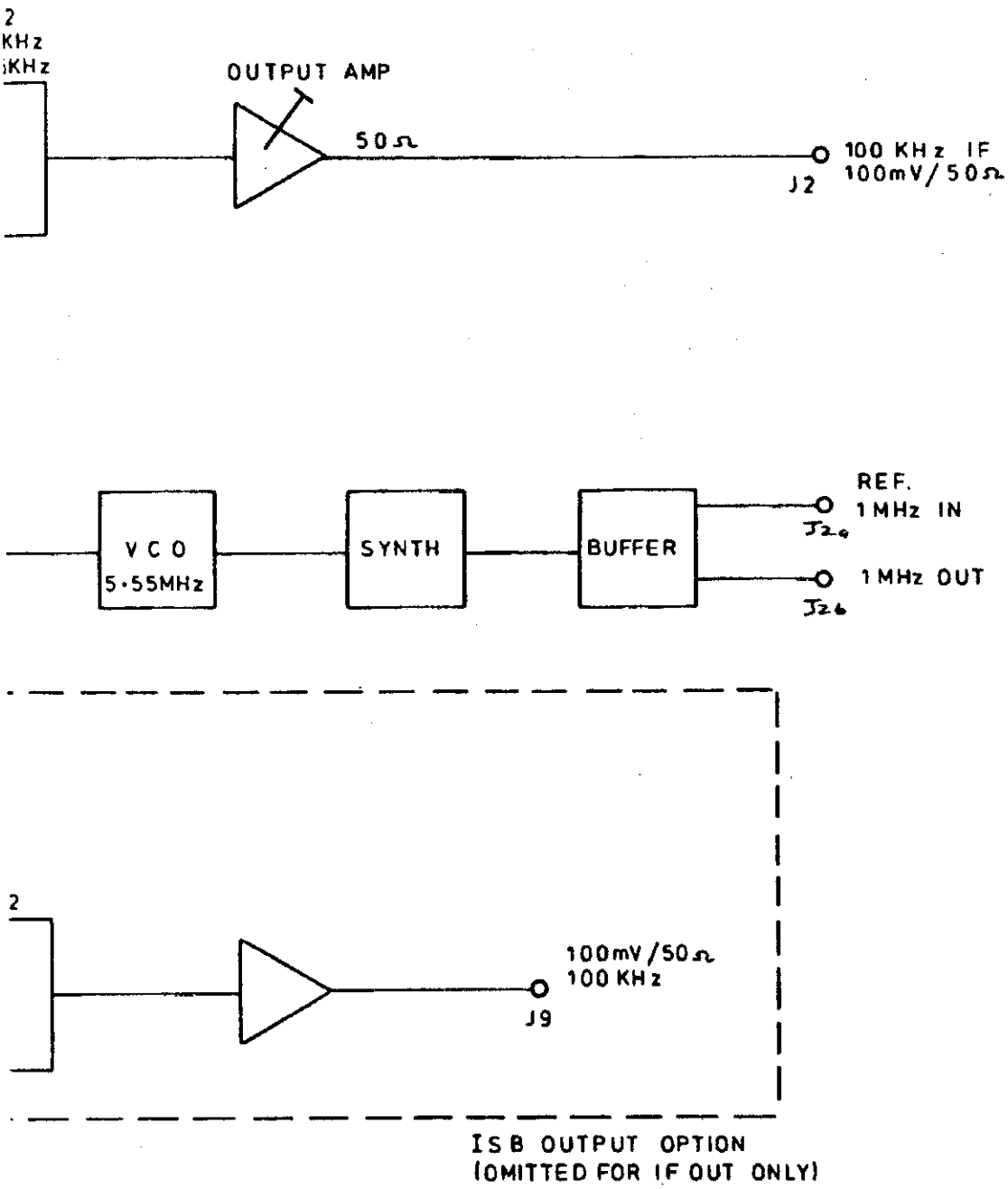



FIG. 1

| RACAL (SLOUGH) LTD. DUKE ST., WINDSOR, BERKS. | | | TITLE FUNCTIONAL BLOCK DIAGRAM | |
|---|---|---|---|---|
| DRN. M.T. 23-9-80. | APP'D. | DATE | ISSUE No. A. | DRG. No. 40-7034 |

# CHAPTER 2

# INSTALLATION

Paragraph


| | |
|---|---|
| 1 | OPTION MODIFICATION KIT |
| 2 | INTRODUCTION |
| 3 | INSTALLATION PROCEDURE |
| 4 | INTERFACE WIRING |

# CHAPTER 2

## 1. OPTION MODIFICATION KIT

### 100kHz IF Output Option

| Description | Quantity | Part No. |
|---|---|---|
| Module | 1 | 51-3001 |
| 1MHz Ref. Cable | 1 | 41-0097 |
| IF Cable | 1 | 41-0096 |
| 6kHz Filter | 1 | |
| PROMS | 3 | |
| Capacitor 330pF | 1 | |
| Capacitor 360pF | 1 | |

### 100kHz IF and ISB Output Option

| | | |
|---|---|---|
| Module | 1 | 51-3002 |
| 1MHz Ref. Cable | 1 | 41-0097 |
| IF Cable | 1 | 41-0096 |
| Output Cable | 1 | 41-0098 |
| 6kHz Filter | 1 | |
| PROMS | 3 | |
| Capacitor 330pF | 1 | |
| Capacitor 360pF | 1 | |

## 2. INTRODUCTION

This chapter contains general installation data and detailed interface wiring requirements. The module is mounted in the rear of the receiver on the pillars intended for the ISB board, A5. If the ISB option is fitted it must be secured to the top of the 100kHz option.

## 3. INSTALLATION PROCEDURE

1) First remove the top and bottom covers from the RA1792 Receiver and remove the mains lead.

2) Take the cableform 41-0097 and carefully thread PL1 and PL2, from the back of the Receiver, underneath the main IF/AF tray, to the front of the Receiver.

3) Mount the 100kHz IF Option box using the four M4 pillars at the rear of the Receiver and secure with the M5X5 bolts.

4) Mount the PCB 49-0122 onto the M3 pillars in the box and secure with four M3 nuts.

5) Solder a wire link from pin 1 of the PCB to the feedthrough capacitor -C.

ISB Option

6) Secure the second PCB 49-0123, component side down, to four pillars on the top of the first PCB.

7) Solder a wire link from pin 3 on the main PCB to pin 1 on the ISB Option PCB.

8) Also included in the modification is the addition of a filter on the main IF/AF board, and the changing of the PROMS on the microcomputer board.

9) On the microcomputer board A6A2, remove the existing PROMS, U5, U6 and U7, and replace with the new PROMS supplied.

10) Remove the main IF/AF board from the Receiver and solder the 6kHz filter in FL5 position.

Also solder the capacitors supplied in the spare holes provided at each end of FL5.

The input capacitor is 360pF and the output capacitor is 330pF.

## 4. INTERFACE WIRING

1) Connect a length of wire between the feedthrough capacitor, C1 on the A2 module of the Receiver, and the feedthrough on the 100kHz IF module.

2) Turn the Receiver on its side and remove the lids from the A7 and A8 modules. Remove the cable linking J2 on A7 to J2 on A8.

   This cable should be stored in case of future use by coiling up and clipping to the cable clip at the rear of the receiver, next to the main IF output socket.

3) Connect PL1 to J2 on A7 and PL2 to J2 on A8. Replace the lids on A7 and A8.

4) Turning to the 100kHz IF module, connect PL3 to J2a and PL4 to J2b on the 100kHz IF board.

5) Disconnect the cable W12P1 from J4 on A4 and reconnect to J3 on the 100kHz board.

6) Connect cable 41-0096 to J4 on A4 and the other end to J4a on the 100kHz board.

### ISB OPTION

7) Use the cable mentioned in operation (2), to connect the main board J1 to the ISB board J2.

8) Use cable 41-0096 to connect the main IF/AF module A4 socket J2 to the ISB board J1a.

9) Connect cable 49-0098 between J3 on the ISB board and fit the BNC bulkhead to the back panel of the RA1792, in the ISB output position.

# CHAPTER 3

# OPERATION

## LOCAL OSCILLATOR SYNTHESISER

The local oscillator is a standard phase locked loop synthesiser producing an output frequency of 555kHz.

The block diagram of the frequency synthesiser is shown in Figure 2

A 1MHz reference is taken from the RA1792 and fed to J2a via a long length of coaxial cable. Due to the long cable the 1MHz signal becomes degraded and so it has to be reconstituted by TR7 and buffered before being fed back to the Receiver synthesiser. This transistor also defines the impedance of the tap such that the effect of the cable is minimised.

IC2d and IC2e convert the signal to a 15 volt square wave which is available on TP5. This 1MHz square wave is divided by 1000 by IC6 and IC7 to produce a 1kHz square wave at TP3. This forms the reference signal for the frequency synthesiser.

A 1kHz waveform also exists on TP6 which is the output of the digital divider. These two signals are fed to a phase sensitive detector whose dc output depends on the difference in phase between the reference input and the divided 1kHz input.

The output is low pass filtered by C10, C6 and R7, to remove any 1kHz reference, and buffered to produce a dc level on TP1. This dc level is the control voltage to a voltage controlled oscillator formed by TR1, L1, C2, D1, and D2.

This is basically an LC oscillator whose frequency is controlled by a dc level changing the capacitance of the two varicap diodes D1 and D2.

The output of the VCO is a 5.55MHz low level sine wave. this signal is buffered by TR3 and subsequently converted to a high level square wave by IC2a and IC2b. Thus at TP2 there is a +15 volt 5.55MHz square wave.

This 5.55MHz square wave is fed to a divider chain consisting of IC4, 8, 10, 12 and IC5. The dividers are programmable devices whose division ratios are set by applying the desired logic level to their program inputs. The divider is programmed to divide by 5550 thus producing a 1kHz signal which is fed into the phase detector.

In operation, IC4 counts the 5.55MHz down to the program count and then produces a carry signal to IC8. IC8 in turn counts down from its program count and feeds a carry out to IC10. IC10 similarly counts down and feeds its carry to one half of IC12. All the carry outputs and the Q output of IC12a are decoded by IC5b and are used to reset the chain. The reset action is performed by IC12b to ensure reliable reset pulses.

The counter devices are LOCMOS devices which are guaranteed to operate at a high enough frequency to ensure reliable operation of the divider.

The 5.55MHz square wave, at TP2, is also fed to IC9. This is a symmetrical divide by 10 operation producing a 555kHz square wave at pin 11 of IC9.

TR4 converts this to a 5 volt square wave which is suitable for driving the 50 ohm drivers of IC11. These produce two outputs each at a level of +7dBm at 50ohm impedance.

The one local oscillator signal is fed to the mixer, X1 of the IF signal path while the second is fed to a coaxial socket, J1. This is used as the local oscillator for the ISB option.

SIGNAL PATH

The IF signal is down converted to 100kHz and amplified to produce an output which is at the same level as the existing 455kHz IF.

The 455kHz IF is taken from the main AF/IF BOARD, A4, and fed to a coaxial socket, J4a on the 100kHz board. The signal is low pass filtered by L2, 3, 4, C1, 3, 5, 8, 11, 12 and C14 and fed to the mixer X1.

The low pass filter is required to prevent the local oscillator signal from getting back into the receiver. Its response is flat, to within 0.5dB, up to 475kHz, and then falls off to provide 60dB attenuation at 555kHz, the local oscillator frequency.

The input and output impedances are 50 ohm, thus matching the IF and the mixer, which are both 50 ohm impedance.

The 100kHz IF is fed from the mixer to another low pass filter comprising, L5, L6, C16, 17, 18, 19 and C20. This filter is flat to within 0.5dB up to 200kHz and then falls off to provide at least 40dB attenuation at frequencies above 455kHz.

This filter protects the IF from the 555kHz local oscillator signal, which is only guaranteed to be attenuated by 40dB in the mixer.

Finally the 100kHz IF is fed, via R19, to a 50 ohm output impedance, buffer amplifier consisting of TR5 and TR6. The input level is adjusted by R19 such that the output is the same as the input at J4a. The amplifier can provide up to 10dB gain to make up for losses in the filters and mixer. The inter-modulation performance of this amplifier is very good such that the performance of the overall receiver is not degraded.

For the ISB option another IF strip is used which is identical in operation to the one just described.

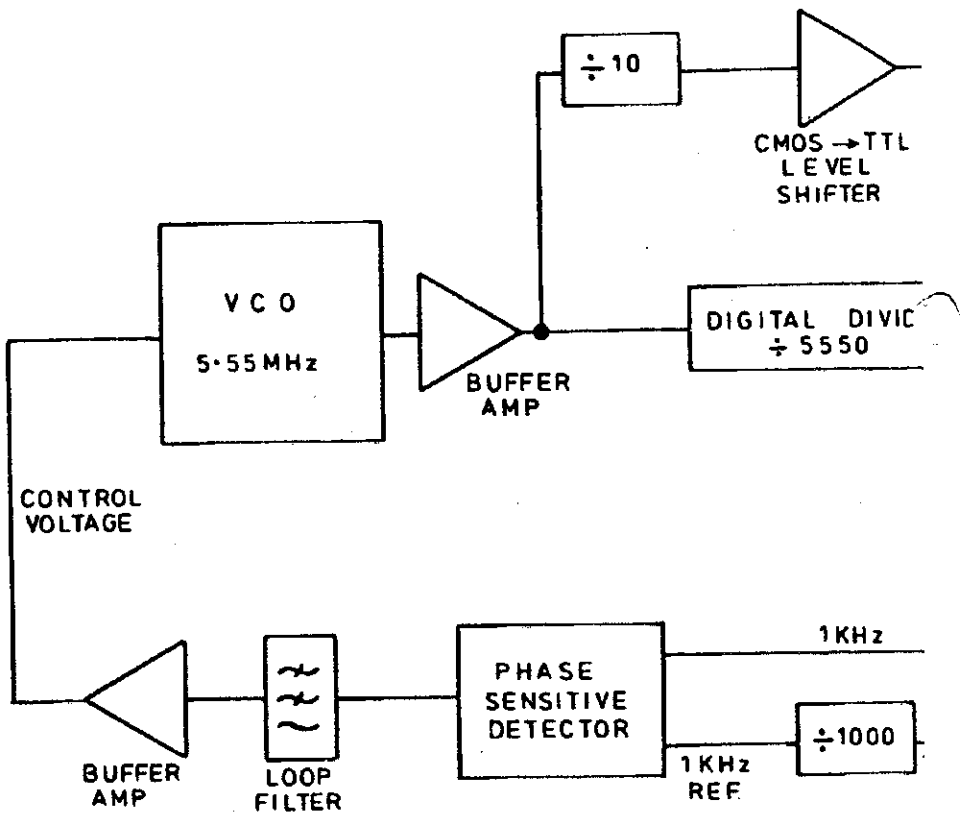
POWER SUPPLY

The power supply is taken from the +15 volt rail in the main receiver. This enters via a feedthrough capacitor and is also filtered by L7, and C36 to ensure that the high level local oscillator signals are not picked up on the supply line to the rest of the receiver.

A 5 volt supply is derived from IC13 to provide a supply for the TTL devices and level converter.

Decoupling is provided on the supply to each I.C.

The whole 100kHz IF board requires approximately 200mA at 15 volts dc.




Admal P/2/1036 2 x A4 SIZE

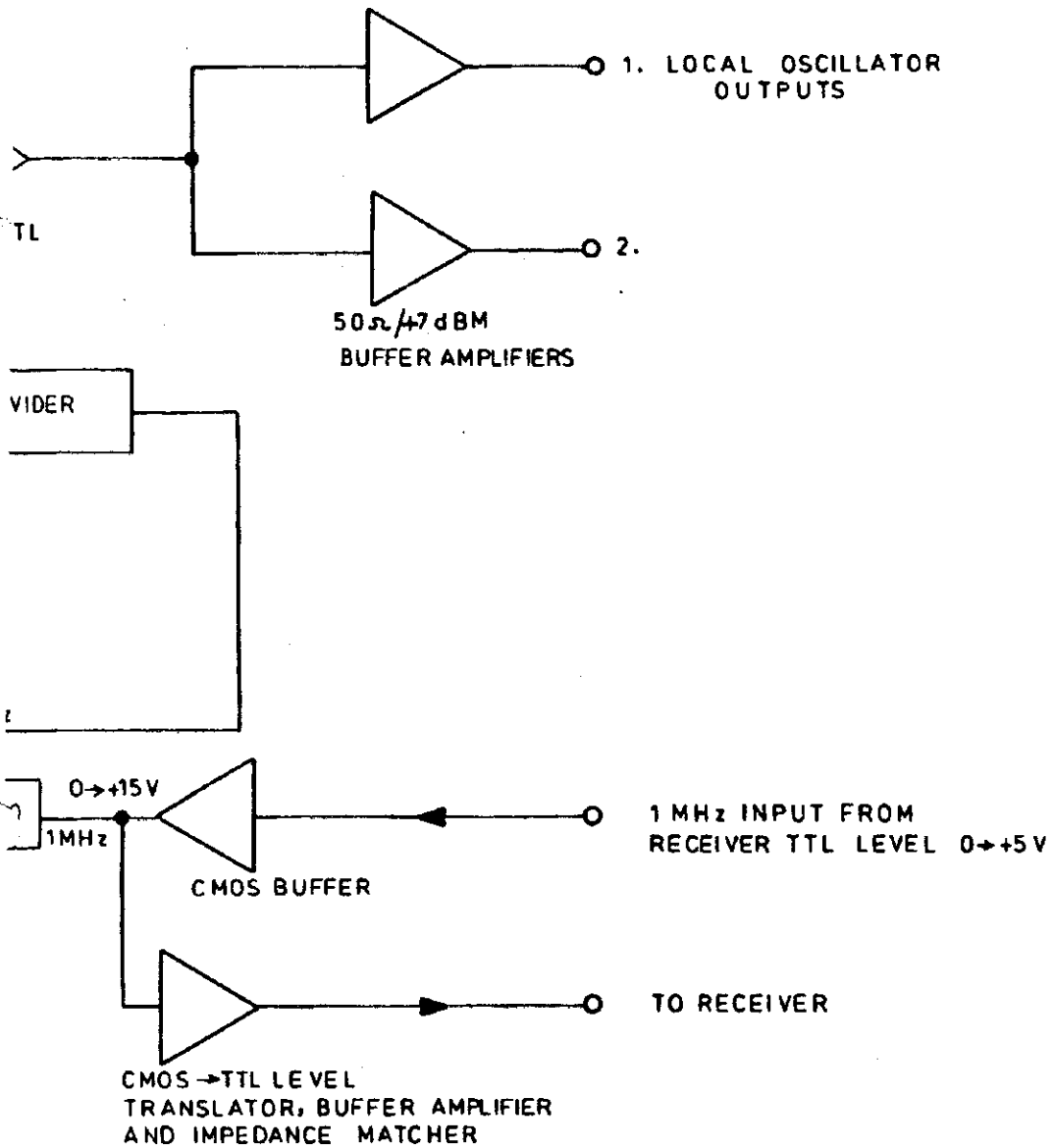



FIG. 2

| RACAL (SLOUGH) LTD. DUKE ST., WINDSOR, BERKS. | | | TITLE FREQUENCY SYNTHESISER BLOCK DIAGRAM. | |
|---|---|---|---|---|
| DRN M.L 23.9.80 | APP'D. | DATE | ISSUE No. a | DRG. No. 40-7034 |

# CHAPTER 4

# ALIGNMENT PROCEDURES

## CONTENTS


| Paragraph | | |
|---|---|---|
| 1 | INTRODUCTION |
| 2 | ALIGNMENT PROCEDURE |


## TABLES


| Table No. | |
|---|---|
| 1 | Test Equipment Required |

# CHAPTER 4

## ALIGNMENT PROCEDURE

### 1. INTRODUCTION

This chapter contains alignment procedures for the 100kHz IF Output Option when fitted to the RA1792 Receiver.

Only the lid to the 100kHz option need be removed in order to align the module.

Table 4-1 lists the test equipment required. Those listed in the example column are recommendations only. Any instruments with equal or better characteristics may be substituted.

Table 4-1

Test Equipment

| Item | Instrument | Specifications | Recommendations |
|---|---|---|---|
| 1 | Digital Multimeter | Range 0-30V dc. | Racal 9077A |
| 2 | Digital Frequency | Range 0 - 10MHz<br>Sensitivity 10mV rms<br>Impedance 1MΩ<br>Accuracy 1 part in $10^6$ $\pm$ 1 count | Racal 9903 |
| 3 | Spectrum Analyser Tracking Generator | Range 1kHz to 100MHz<br>BW 10Hz | Hewlett-Packard 8552B/8553B/ 8443A/141T |
| 4 | High Impedance Probe | Response $\pm$0.5dB 0.1 to 110MHz | H.P. 1121A |
| 5 | | 50Ω LOAD | |

## 2. ALIGNMENT PROCEDURE

1. With the 100kHz option fitted and the Receiver power supply switched on, attach the frequency counter, item 2 to TP5.
   Check that the frequency at TP5 is 1kHz.
   Remove the frequency counter.

2. Place the DVM on TP1 set to 30V dc range.
   Adjust L1 for a level of 7V.
   Remove the DVM from TP1.

3. Connect the frequency counter to J1 and check for a signal of frequency 555kHz.
   If not re-check the setting of L1.
   Remove the frequency counter from J1.
   Switch receiver OFF.

4. Connect the tracking generator, item 3, to J4, at a level of -10dBm.
   Connect the spectrum analyser to the junction of C12/C14 via a 50 ohm coaxial lead.
   SET ANALYSER TO:-

| FUNCTION | SETTING |
|---|---|
| BW | 3kHz |
| Scan Width | 100kHz/DIV |
| Datum | 500kHz |
| Vertical scale | 10dB/DIV |

   Check for response of first filter:-

| | |
|---|---|
| Passband attn. | < 0.5dB |
| Passband ripple | < 0.5dB |

   Referring to Figure 3
   Adjust L2 to obtain notch at 990kHz
   Adjust L3 to obtain notch at 630kHz
   Adjust L4 to obtain notch at 556kHz

Connect the analyser input to J4b on the 100kHz board, using a high impedance probe.
The analyser should show a signal at 455kHz - the standard RA1792 IF.
Take note of the level of this IF and also its harmonic levels.

10. Now place the high impedance probe on the junction of C23/R26 and note the 100kHz IF signal.
Turn R19 clockwise; thus reducing the output level.
Now increase the output level, by turning R19 anti-clockwise, until it is the same as that of the previously measured 455kHz signal.
Careful adjustment of R19 is required to prevent the harmonic content from getting larger than the 455kHz harmonics.

11. Remove the 50 ohm load from the RA1792 and replace the lid on the 100kHz IF Output Option.

ISB Option

If the ISB option is fitted, repeat operations 4 - 11 inclusive, for the ISB IF Board.

FIGURE 3 100KHz I.F. INPUT FILTER

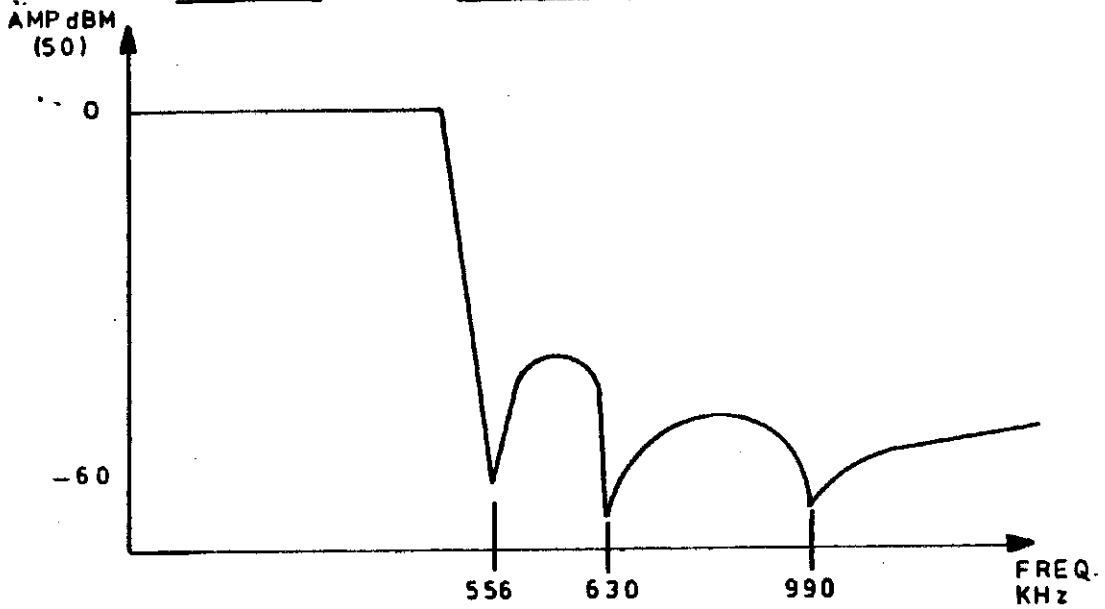
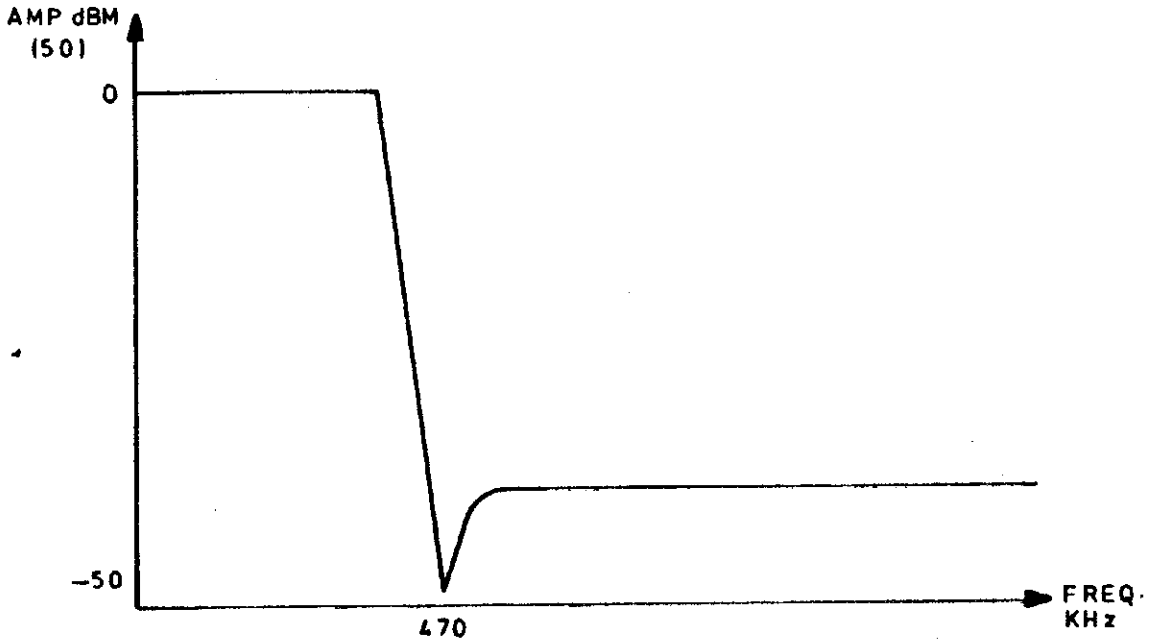



FIGURE 4 100KHz I.F. OUTPUT FILTER




| | | | | |
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| RACAL (SLOUGH) LTD. DUKE ST., WINDSOR, BERKS. | | | TITLE FIGURES 3 AND 4 | |
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ADMEL 5135C

A4 SIZE

# CHAPTER 5

# COMPONENTS LISTS

## 1. INTRODUCTION

This chapter contains the component lists for the 100kHz IF Output Option for the RA1792 Receiver.

The components are arranged in sequences by unit designation.

ASSEMBLY OF 100kHz IF OPTION

| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| Capacitors | | | | | |
| C1 | 4,400p | Polystyrene | | ±2% | |
| C2 | 10p | Ceramic | | | |
| C3 | 1,300p | Polystyrene | | ±2% | |
| C4 | 0.1µ | Ceramic | | | |
| C5 | 7,600p | Polystyrene | | ±2% | |
| C6 | 0.33µ | Polyester | | ±10% | |
| C7 | 150p | Ceramic | | | |
| C8 | 7,000p | Polystyrene | | ±2% | |
| C9 | 0.1µ | Ceramic | | | |
| C10 | 1µ | " | | | |
| C11 | 6,600p | Polystyrene | | ±2% | |
| C12 | 5,600p | " | | " | |
| C13 | 330p | Ceramic | | | |
| C14 | 1,900p | Polystyrene | | ±2% | |
| C15 | 0.1µ | Ceramic | | | |
| C16 | 19,600p | Polystyrene | | ±2% | |
| C17 | 920p | " | | " | |
| C18 | 31,000p | " | | " | |
| C19 | 2,500p | " | | " | |
| C20 | 18,000p | " | | " | |
| C21 | 0.1µ | Ceramic | | | |
| C22 | 330p | Polystyrene | | ±2% | |
| C23 | 0.1µ | Ceramic | | | |
| C24 | 0.1µ | " | | | |
| C25 | 4.7µ | Tantalum | | | |
| C26 | 68µ | " | | | |
| C27 | 0.1µ | Ceramic | | | |
| C28 | 0.1µ | " | | | |
| C29 | 0.1µ | " | | | |
| C30 | 0.1µ | " | | | |
| C31 | 0.1µ | " | | | |
| C32 | 0.1µ | " | | | |
| C33 | 0.1µ | " | | | |
| C34 | 0.1µ | " | | | |
| C35 | 0.1µ | " | | | |
| C36 | 150p | Ceramic | | | |

| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| **Diodes** | | | | | |
| D1 | | MV2302 | | | |
| D2 | | " | | | |
| D3 | | HP5082-2800 | | | |
| D4 | | DPA050 | | | |
| D5 | | IN4148 | | | |
| D6 | | " | | | |
| **Integrated Circuits** | | | | | |
| IC1 | | 78M06HC | | | |
| IC2 | | HEF4049B | | | 32-4368 |
| IC3 | | 410164 | | | |
| IC4 | | HEF4516BP | | | 32-4491 |
| IC5 | | HEF4002BP | | | 32-4361 |
| IC6 | | HEF4040BP | | | |
| IC7 | | HEF4068BP | | | |
| IC8 | | HEF4516BP | | | |
| IC9 | | HEF4520BP | | | |
| IC10 | | HEF4516BP | | | |
| IC11 | | SN74S140 | | | |
| IC12 | | HEF4013BP | | | 32-4362 |
| IC13 | | 7805UC | | | 32-4405 |
| **Inductors** | | | | | |
| L1 | | T6356 | | | 47-5008 |
| L2 | | T7307 | | | 47-3003 |
| L3 | | T7308 | | | 47-3004 |
| L4 | | T7309 | | | 47-3005 |
| L5 | | T7310 | | | 47-3006 |
| L6 | | T7311 | | | 47-3007 |
| L7 | 100µH | R.F. Choke | | | |

| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| Resistors | | | | | |
| R1 | 15K | Metal oxide | ¼W | ±5% | 30-4235 |
| R2 | 82K | " " | " | " | 30-4243 |
| R3 | 100Ω | " " | " | " | 30-4210 |
| R4 | 1.5K | " " | " | " | 30-4223 |
| R5 | 10Ω | " " | " | " | 30-4111 |
| R6 | 2.2K | " " | " | " | 30-4226 |
| R7 | 2.2K | " " | " | " | " " |
| R8 | 1.5K | " " | " | " | 30-4223 |
| R9 | 1.5K | " " | " | " | " " |
| R10 | 270K | " " | " | " | 30-4156 |
| R11 | 100K | " " | " | " | 30-4240 |
| R12 | 270K | " " | " | " | 30-4156 |
| R13 | 68Ω | " " | " | " | 30-4208 |
| R14 | 68Ω | " " | " | " | " " |
| R15 | 10Ω | " " | " | " | 30-4111 |
| R16 | 47K | " " | " | " | 30-4239 |
| R17 | 4.7K | " " | " | " | 30-4135 |
| R18 | 15K | " " | " | " | 30-4235 |
| R19 | 5K | Potentiometer | | | 30-7140 |
| R20 | 100K | Metal Oxide | ¼W | ±5% | |
| R21 | 12K | " " | " | " | 30-4234 |
| R22 | 1K | " " | " | " | 30-4220 |
| R23 | 1K | " " | " | " | " " |
| R24 | 10K | " " | " | " | 30-4233 |
| R25 | 390Ω | " " | " | " | 30-4214 |
| R26 | 39Ω | " " | " | " | 30-4206 |
| R27 | 470Ω | " " | " | " | 30-4215 |
| R28 | 10K | " " | " | " | 30-4233 |
| R29 | 470Ω | " " | " | " | 30-4215 |
| R30 | 220Ω | " " | " | " | |

| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| **Transistors** | | | | | |
| TR1 | | BFW10 | | | |
| TR2 | | 2N4338 | | | |
| TR3 | | BCY70 | | | 32-6212 |
| TR4 | | 2N2369 | | | 32-6205 |
| TR5 | | 2N5089 | | | 938417 |
| TR6 | | 2N5089 | | | 938417 |
| TR7 | | 2N2369 | | | 32-6205 |
| **Sockets** | | | | | |
| J1 | | SMB | | | |
| J2a | | " | | | |
| J2b | | " | | | |
| J3 | | " | | | |
| J4a | | " | | | |
| J4b | | " | | | |
| **Mixer** | | | | | |
| X1 | | 1793 | | | |

## ASSEMBLY OF 100kHz ISB IF OPTION

| Cct. Ref. | Value | Description | Rat. | Tol. % | Racal Part Number |
|---|---|---|---|---|---|
| **Capacitors** | | | | | |
| C1 | 4,400p | Polystyrene | | ±2% | |
| C2 | 1,300p | " | | " | |
| C3 | 7,600p | " | | " | |
| C4 | 7,000p | " | | " | |
| C5 | 6,600p | " | | " | |
| C6 | 5,600p | " | | " | |
| C7 | 1,900p | " | | " | |
| C8 | 19,600p | " | | " | |
| C9 | 920p | " | | " | |
| C10 | 31,000p | " | | " | |
| C11 | 2,500p | " | | " | |
| C12 | 18,000p | " | | " | |
| C13 | 0.1µ | Ceramic | | ±20% | |
| C14 | 0.1µ | " | | " | |
| C15 | 0.1µ | " | | " | |
| C16 | 0.1µ | " | | " | |
| **Inductors** | | | | | |
| L1 | | T7307 | | | 47-3003 |
| L2 | | T7308 | | | 47-3004 |
| L3 | | T7309 | | | 47-3005 |
| L4 | | T7310 | | | 47-3006 |
| L5 | | T7311 | | | 47-3007 |
| **Resistors** | | | | | |
| R1 | 5K | Variable | ¼W | ±5% | 30-7140 |
| R2 | 12K | Metal oxide | " | " | 30-4234 |
| R3 | 1K | " " | " | " | 30-4220 |
| R4 | 10K | " " | " | " | 30-4223 |
| R5 | 390Ω | " " | " | " | 30-4214 |
| R6 | 39Ω | " " | " | " | 30-4206 |
| R7 | 47Ω | " " | " | " | |

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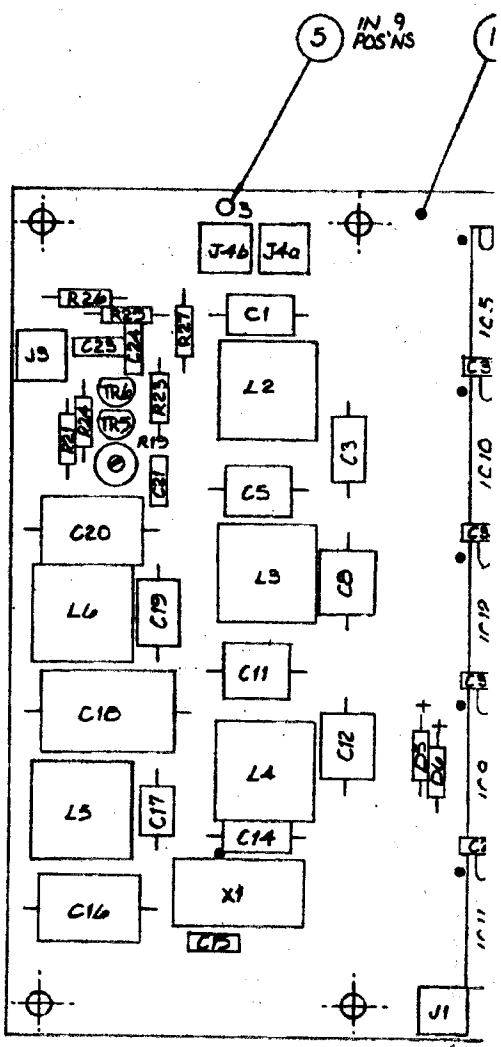
| SECURITY CLASSIFICATION | |
| SERVICE DRAWING No./SHT. No. | |

3rd ANGLE PROJECTION

METRIC / IMPERIAL

USED ON
SI-3001
SI-3002

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| DRAWN R STERRY | |

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RACAL SLOUGH A1 SB

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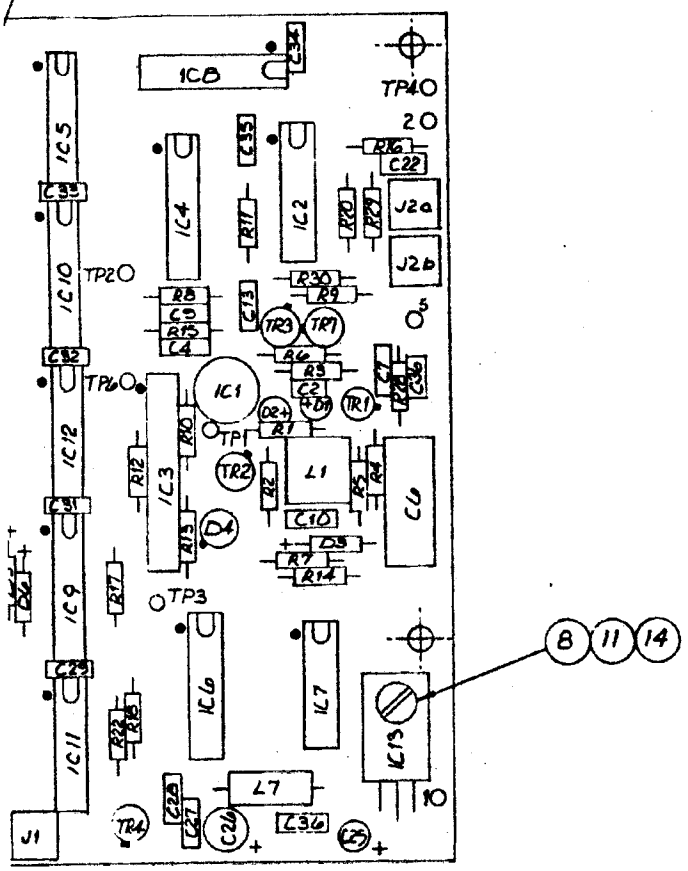


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| SCALE 2/1 | | SERVICE DRAWING No/SHT No SHT 1 OF 1 |

| 1 | 2 | 3 | 4 | 5 | 6 |
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SECURITY CLASSIFICATION

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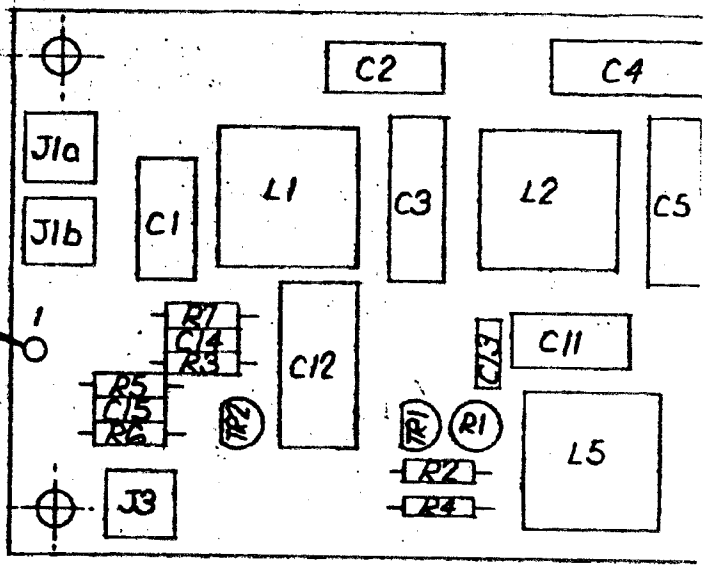
USED ON
51-3002

3rd ANGLE PROJECTION

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| DRAWN R.STERRY | CHANGE | 1 | 13-000 | DIMS. IN | SCALE 2/1 | |
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RACAL SLOUGH A2 DB.

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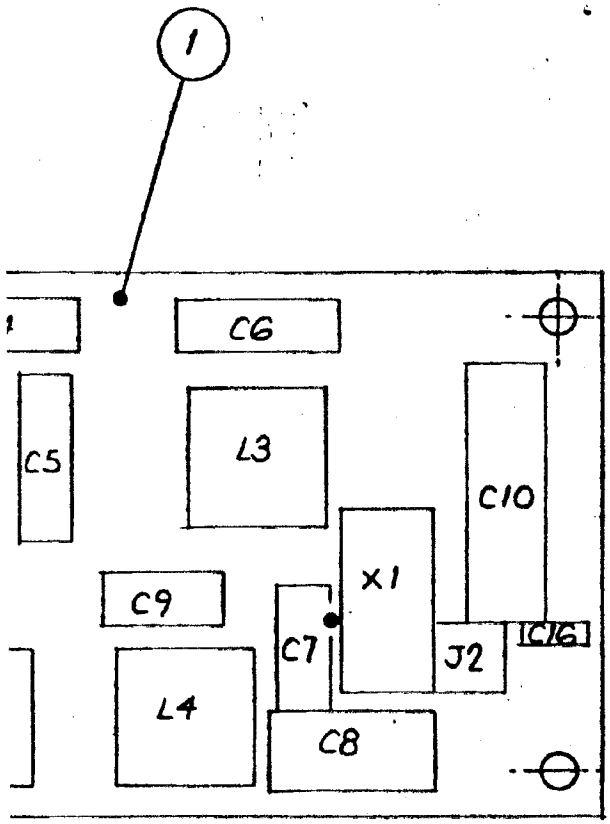


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RACAL DRG. No. 49-0123 SHT 1 OF 1

SERVICE DRAWING No/SHT. No.

A2

ASSEMBLY OF
ISB/IF PCB

| 1 | 2 | 3 | 4 | 5 | 6 |
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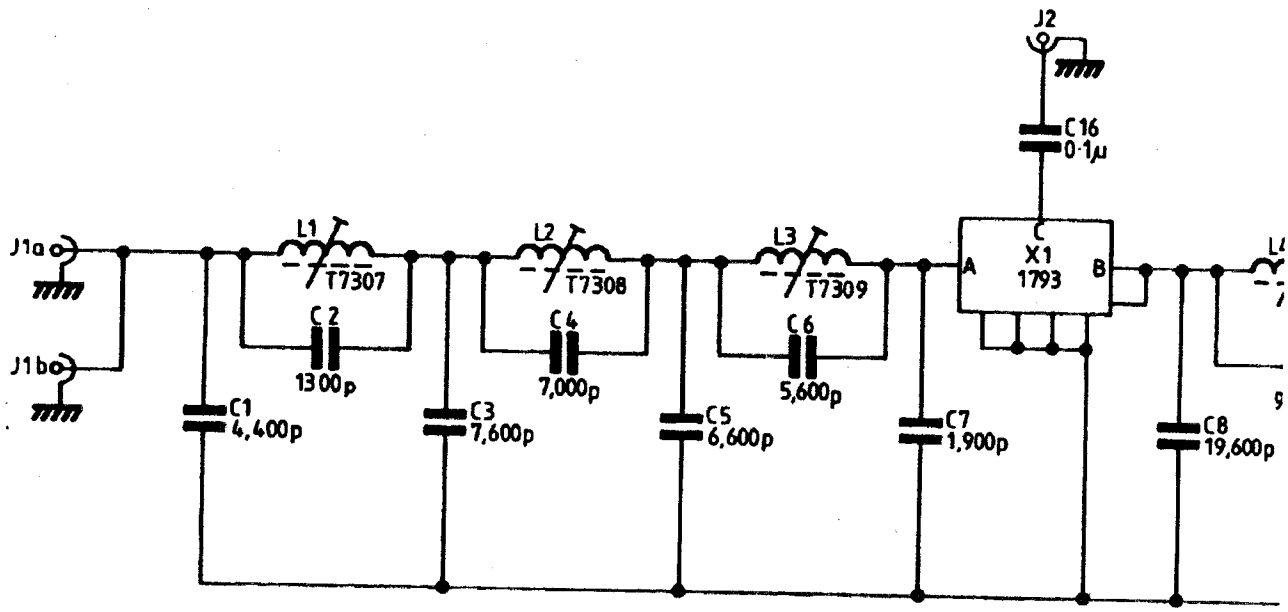
SECURITY CLASSIFICATION

SERVICE DRAWING No./SHT. No.

USED ON
49-0123

3rd ANGLE PROJECTION

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| APP'D | | | | | | |
| CHECKED | | | | FINISH | SURFACE ROUGHNESS | TITLE |
| DRAWN C.F. 8/8/80 | | 1 | 8/8/80 | | | |
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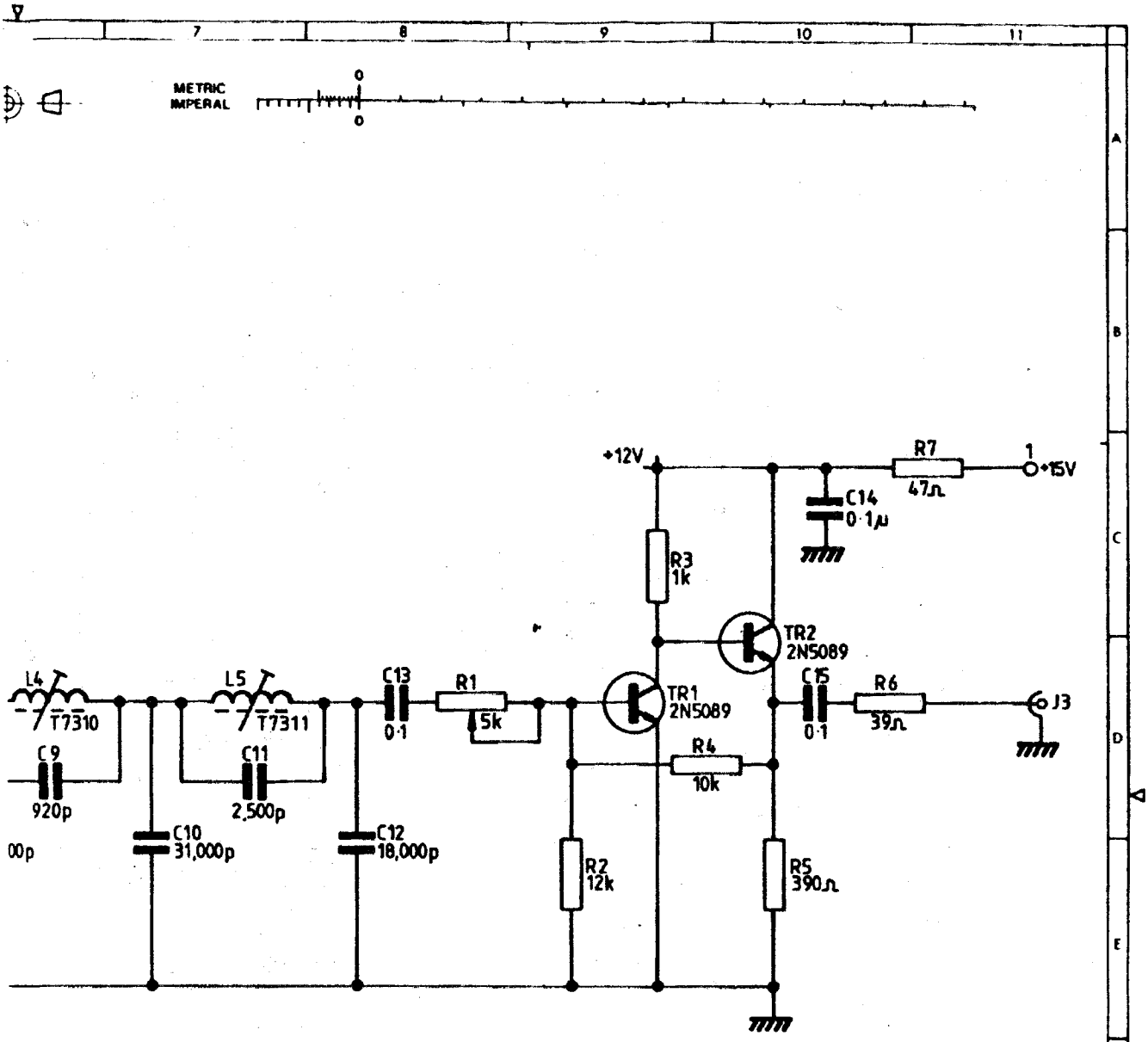
RACAL SLOUGH A2 DB.

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IEET, WINDSOR, BERKS

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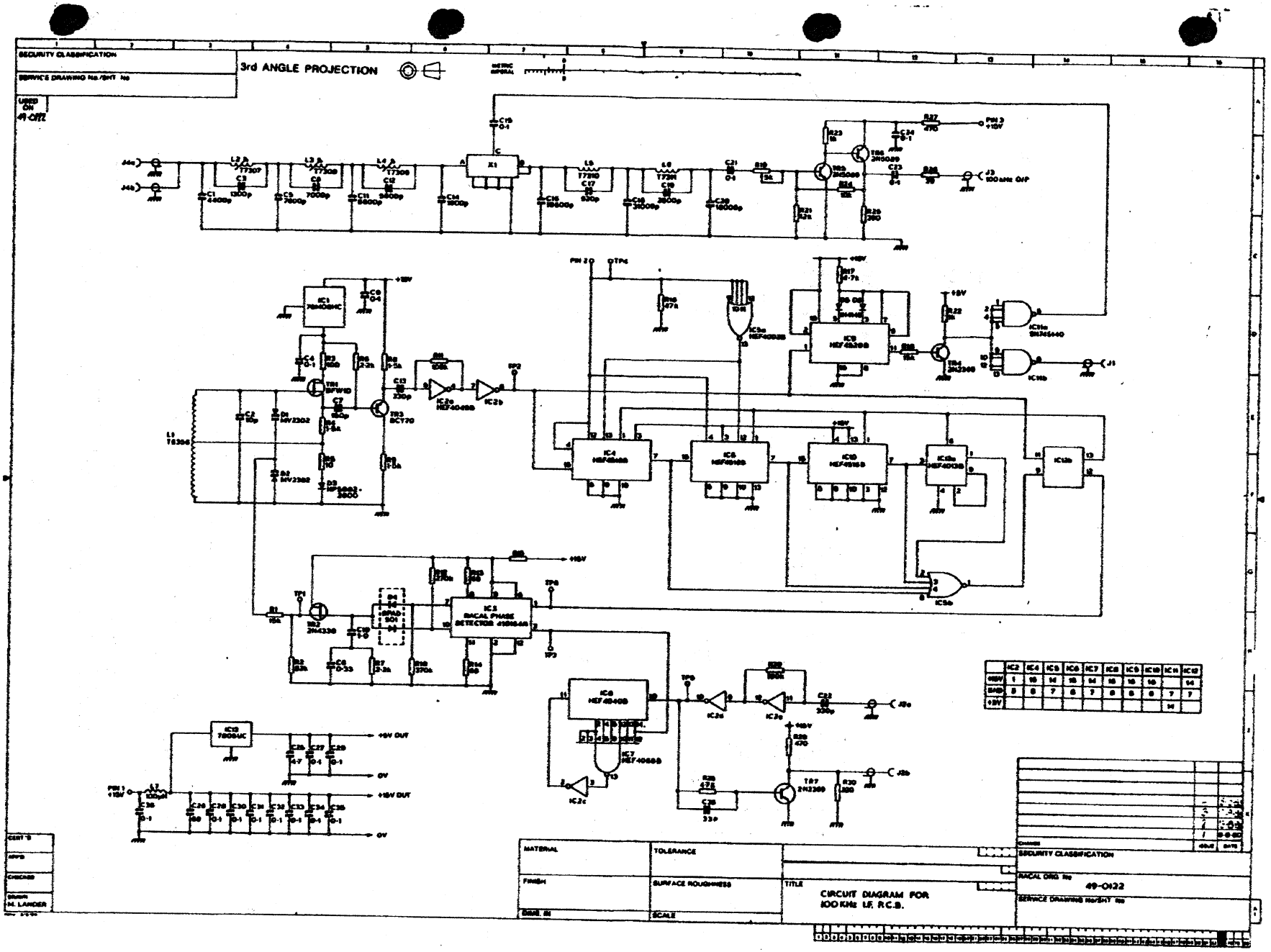
RACAL DRG. No.
49-0123

SERVICE DRAWING No/SHT. No.

A2

CIRCUIT DIAGRAM
FOR ISB/I F PCB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SERVICE'S DRAWING No./SHT. No
3rd ANGLE PROJECTION
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IMPERIAL
USED ON
41-0122
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IC2 HEF4538B
IC3 HEF4538B
IC4 HEF4538B
IC5 HEF4518B
IC6 HEF4518B
IC7 HEF4068B
IC8 HEF4518B
IC9 7808UC
IC10 HEF4518B
IC11 HEF4013B
IC12 SN74S40
IC13 SN74S40
IC14 HEF4011B
IC15 HEF4011B
IC16 HEF4011B
IC17 HEF4011B
IC18 HEF4011B
IC19 HEF4011B
IC20 HEF4011B
IC21 HEF4011B
IC22 HEF4011B
IC23 HEF4011B
IC24 HEF4011B
IC25 HEF4011B
IC26 HEF4011B
IC27 HEF4011B
IC28 HEF4011B
IC29 HEF4011B
IC30 HEF4011B
IC31 HEF4011B
IC32 HEF4011B
IC33 HEF4011B

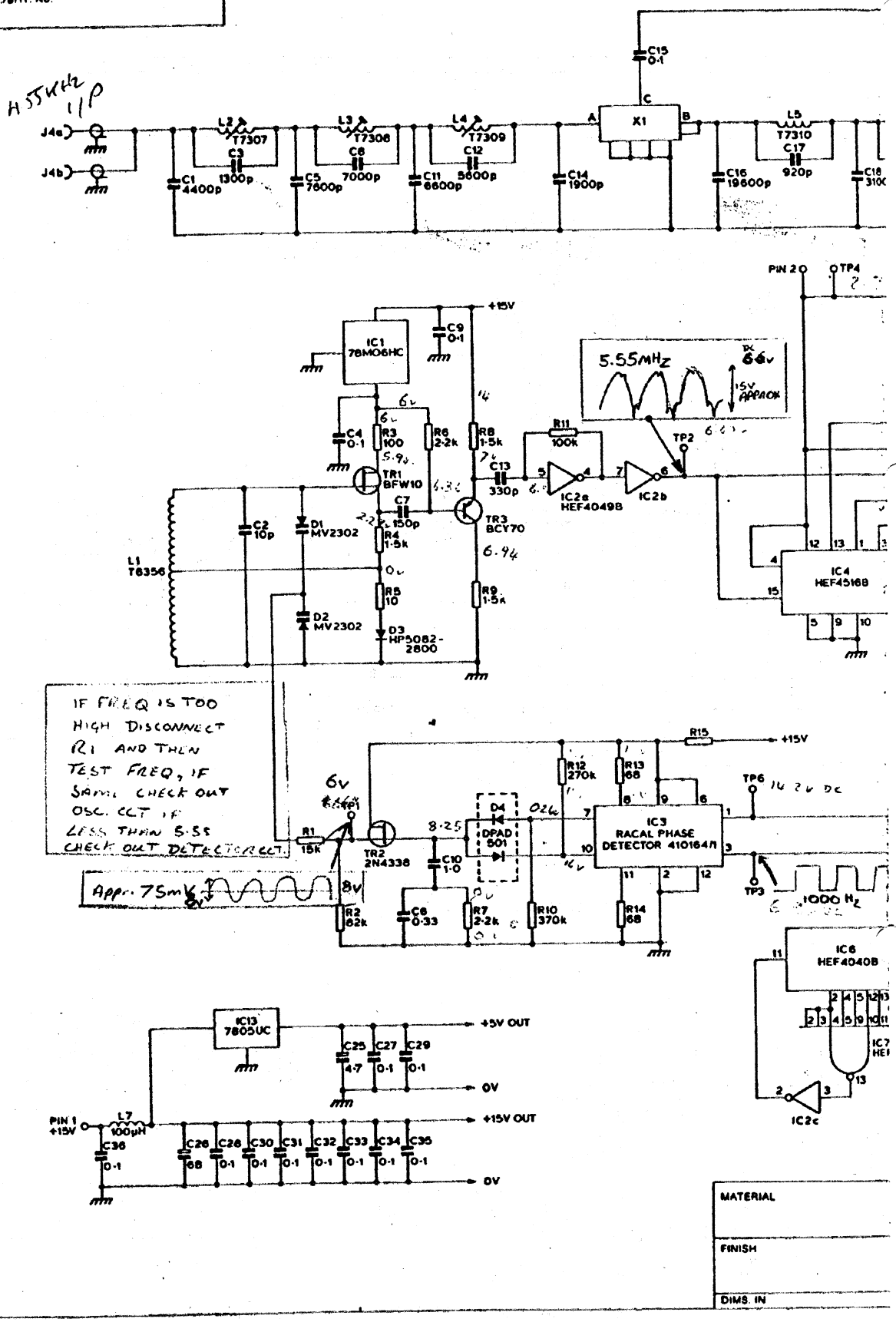
SECURITY CLASSIFICATION

SERVICE DRAWING No./SHT. No.

3rd ANGLE PROJECTION

METRIC IMPERIAL

49-0122

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| CERT'D | |
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| DRAWN | M. LANDER |

MATERIAL

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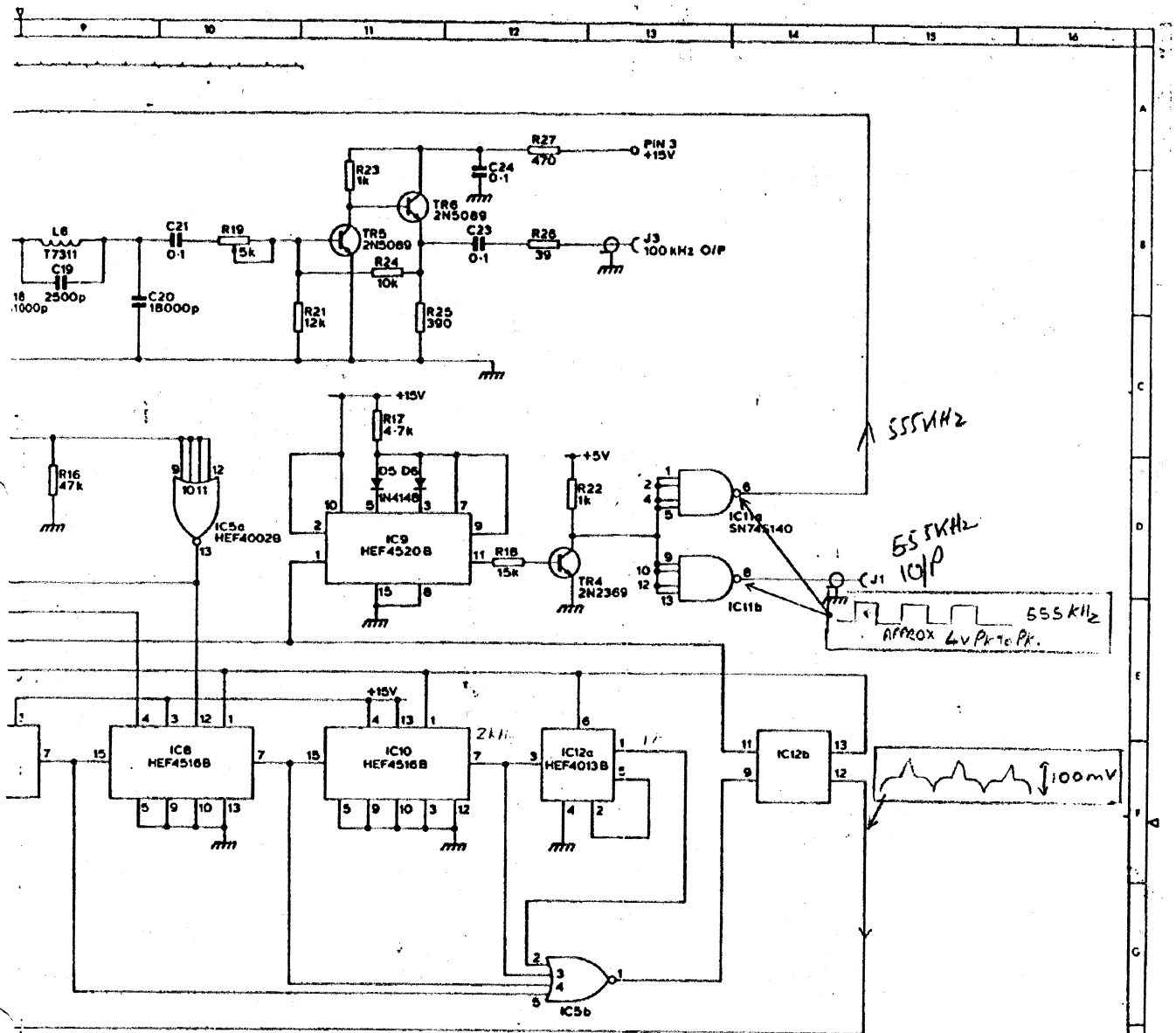
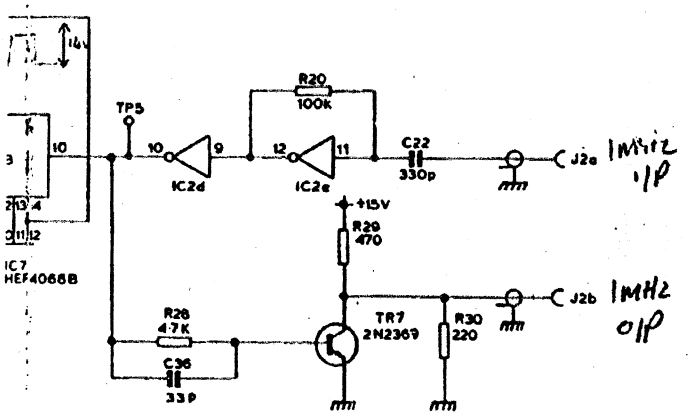
RACAL SLOUGH A1 06.




| | IC2 | IC4 | IC5 | IC6 | IC7 | IC8 | IC9 | IC10 | IC11 | IC12 |
|---|---|---|---|---|---|---|---|---|---|---|
| +15V | 1 | 16 | 14 | 16 | 14 | 16 | 16 | 16 | | 14 |
| GND | 8 | 8 | 7 | 8 | 7 | 8 | 8 | 8 | 7 | 7 |
| +5V | | | | | | | | | 14 | |

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| | 1 | 6-8-80 |

TOLERANCE

SURFACE ROUGHNESS

SCALE

RACAL (SLOUGH) LTD
DUKE STREET, WINDSOR, BERKS

TITLE
CIRCUIT DIAGRAM FOR
100 KHz I.F. P.C.B.

SECURITY CLASSIFICATION

RACAL DRG No
49-0122

SERVICE DRAWING No/SHT No

A1

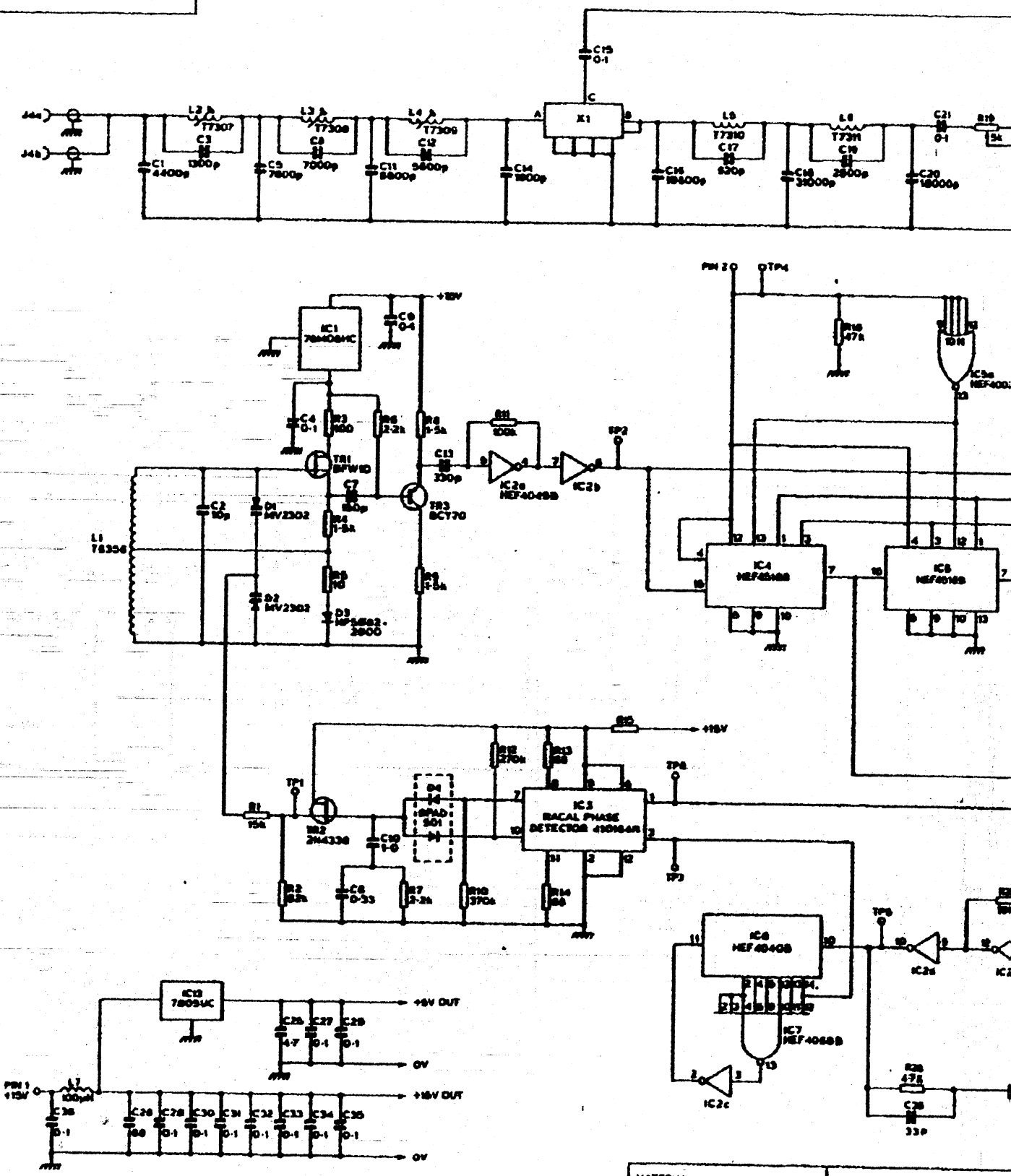
SECURITY CLASSIFICATION

SERVICE DRAWING No./SHT No

3rd ANGLE PROJECTION

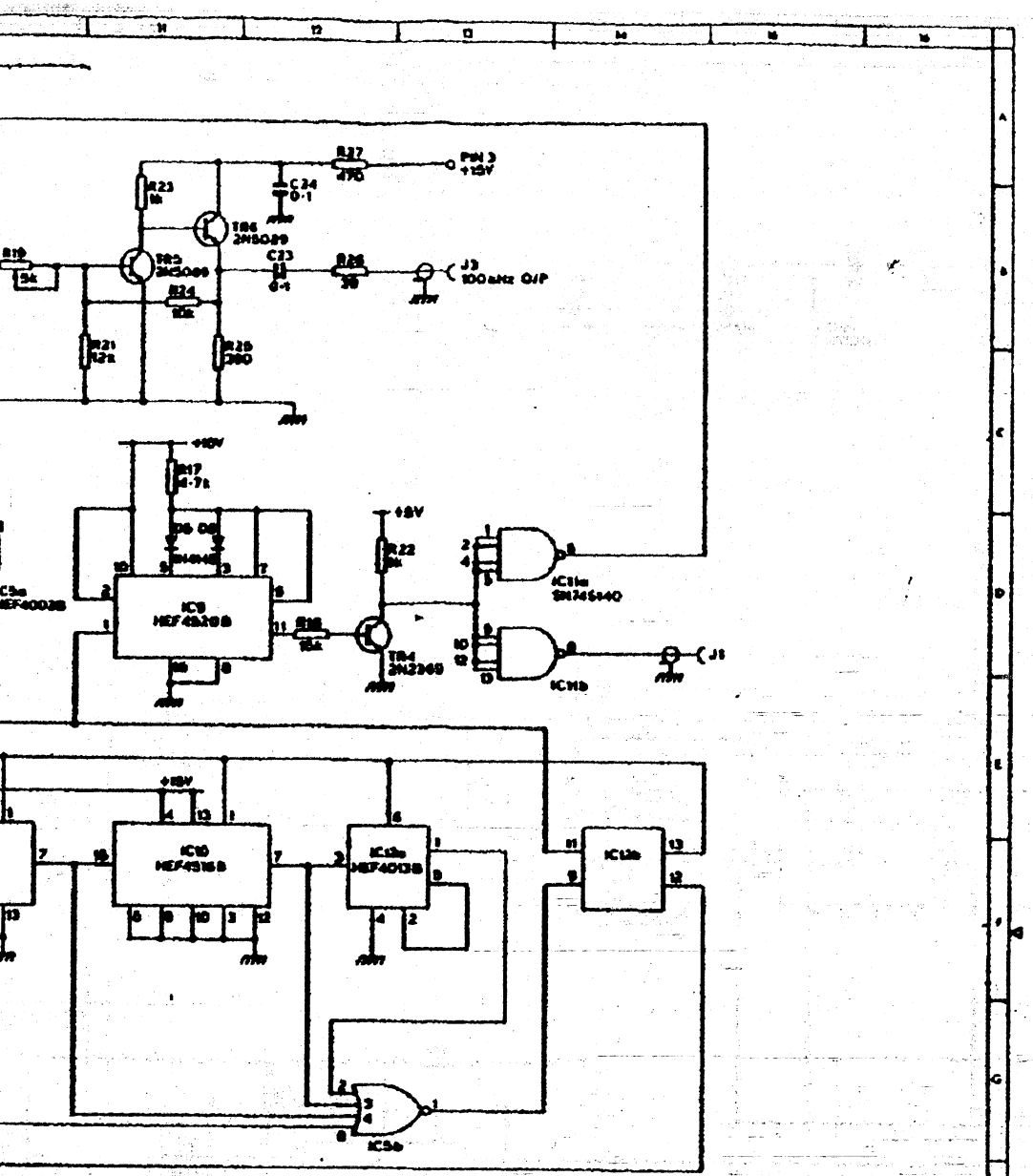
METRIC / IMPERIAL

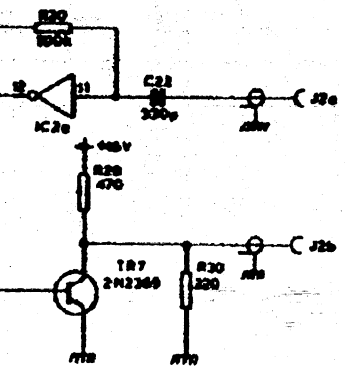
USED ON 41-0112




| | |
|---|---|
| CERT'D | |
| APP'D | |
| CHECKED | |
| DRAWN M. LANDER | |

| | |
|---|---|
| MATERIAL | TOLERANCE |
| FINISH | SURFACE ROUGHNESS |
| DWG. No. | SCALE |




| | IC2 | IC4 | IC5 | IC6 | IC7 | IC8 | IC9 | IC10 | IC11 | IC12 |
|---|---|---|---|---|---|---|---|---|---|---|
| +10V | 1 | 16 | 14 | 16 | 14 | 16 | 16 | 16 | | 14 |
| GND | 8 | 8 | 7 | 8 | 7 | 8 | 8 | 8 | 7 | 7 |
| +5V | | | | | | | | | 14 | |

| CHANGE | ISSUE | DATE |
|---|---|---|
| | 1 | 8-8-80 |

SECURITY CLASSIFICATION

RACAL ORIG No

49-0122

SERVICE DRAWING No/SHT No

TITLE

CIRCUIT DIAGRAM FOR
100 KHz I.F. P.C.B.